Do you really know how to do JESD78 latch-up testing?

Preview of topics for our new user guide.

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ESD Association

Introduction

- **Latch-up testing is not like ESD HBM or ESD CDM testing**
- **Requires more knowledge of the product**
- **JESD78 working group has worked hard to make the test thorough and accurate**
- **Last year, the Industry Council on ESD released a survey**
  - **Showing how the user community had concerns and**
  - **Customers were not certain to the test's effectiveness in some applications**
  - **One conclusion was that there should be a User Guide**
- **JESD78 Working Group will give an overview of topics that will be discussed**

Outline

- Setting up a LUP Test Program
- Power Supply Assignments
- Special Pins
- Maximum Junction Temperature – Calculate and Monitor
- I-Test versus E-Test – Which to Use?
- Tester Calibration
- Waveform Measurements / Calibration
- Pre & Post Voltage/Current Bias/Clamp Levels on Pulse Supply
- Maximum Stress Voltage (MSV)
- Latches in Power Clamps
- Hardware for Testing of HV products
- Testing of SOI, GaN and other products
- Data Review & Analysis
- Destructive vs. Non-Destructive Latch-up

Setting up a LUP Test Program

- Pin continuity testing (at beginning and end)
- Power up/down sequence
- Pin assignment (Input, Output, Supply, or Ground)
  - Decision flow
  - Special pins (see dedicated section)
- Validating the test program
  - IDD checks (with Input pins at High, Low, or Float)
  - Powered Curve-Trace to check signal pin assignment (Input vs. Output)
- Failure detection
- Compare before vs. after LUP stress:
  - Curve-Trace (unpowered/powered)
  - IDD measurements
  - Standard tester datalogs

Power Supply Assignments

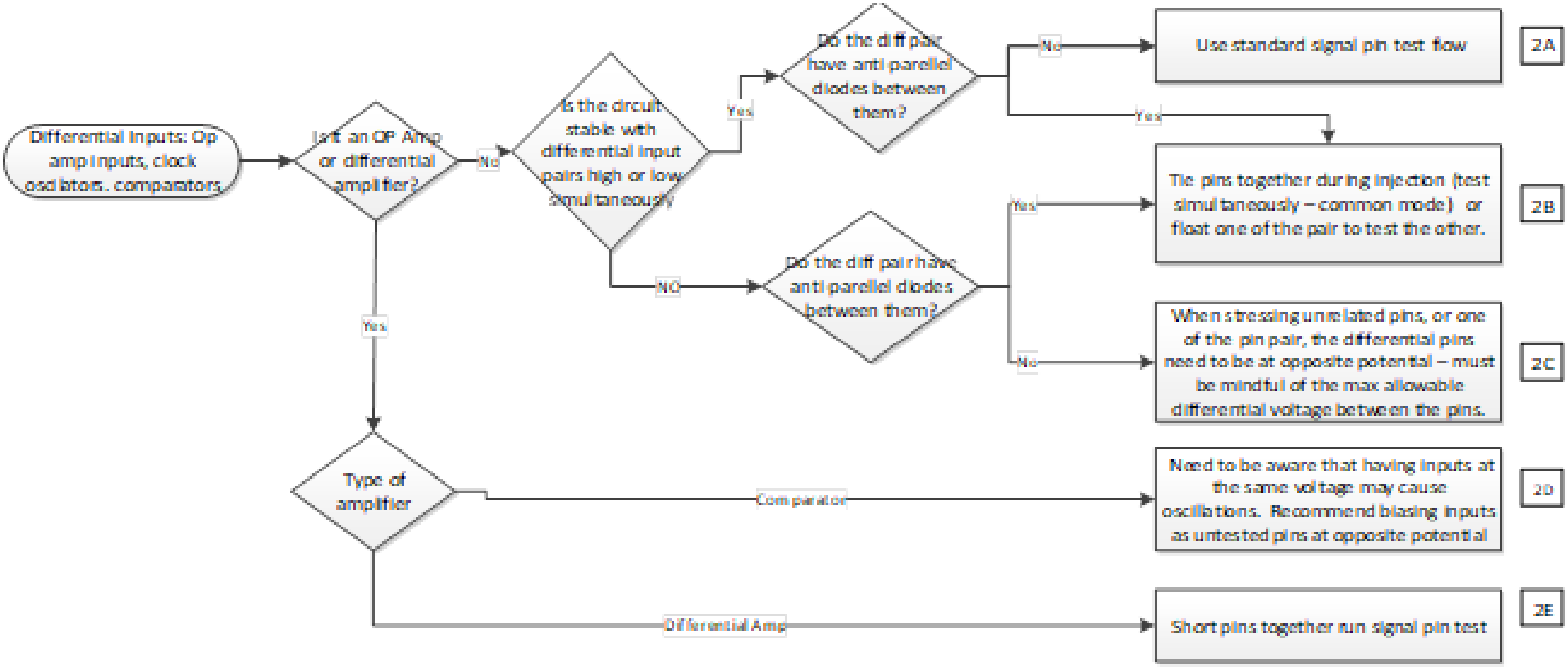
- **Issue:**
  - **In most test systems, there are insufficient power supplies to provide power individually to each supply pin (group)**
  - **Grouping of supply pins (groups) allows efficient power supplies allocation**
  - **However, some care must be taken so LU detection will not be compromised**

- **User Guide Coverage (ref: JESD78F.01, sec 5.4):**
  - **Guidance and examples how to set tester power supplies when**
    - **Sets of pins with the same V_{maxOP} (V_{minOP}) with large variances in current draw should be separated**
    - **Lessens possible masking of latch-up on the lower current draw pins**
    - **Sets of pins with the same V_{maxOP} (V_{minOP}) with small or no variances in current draw can be combined if not enough supplies available**
  - **Throughout testing, all supplies used must be monitored**
    - **All currents and voltages both before and after testing to ensure MSV is correct**

Special Pins

- **Issue -- CMOS/BiCMOS devices have become increasingly complex in the types of circuits contained in any individual device**
  - **Many require engineering effort to determine the proper manner to set up and perform latch-up testing**
  - **Products contain individual pins that do not fit cleanly into the categories**
  - **Pins may require unique pre-configuration or special data assessment methods to properly perform latch-up testing**
- **User Guide Coverage: Special Pins from Annex A provide guidance**
  - **To support testing these non-standard pin types/configurations**
  - **More detailed guidance is planned for the JESD78 User Guide**
  - **The JESD78F.01 Annex A is not expected to address every possible special pin case**
  - **So, we are soliciting inputs on special cases not currently addressed**

Special Pins -- Flowchart



Maximum Junction Temperature – Calculate and Monitor

- **Why use junction temperature?**
  - **Bipolar latch-up occurs at the junction level, typically between wells and substrate**
  - **Latch-up can occur anywhere on the die;**
    - **Varies spatially across the die and**
    - **Is highly temperature dependent**
    - **Highest T_j on the die during field operation ($T_j$max) should be used**
- **User Guide coverage:**
  - **Explain temperature measuring and monitoring techniques**
  - **Methods to convert from junction to case and ambient temperatures**
  - **Describe information necessary to calculate between junction, case and ambient**
    - **Heat transfer of package using θja and θjc plus power consumption of product**

Current Compliance in Voltage Sources

- **Issue:**
  - Latch-up testing requires one or more power supplies
  - Need to set voltage value AND current compliance for each supply
  - What compliance level to set?
  - What to do when current compliance is reached?
    - A test with a voltage supply in compliance is not valid
- **User Guide Coverage:**
  - Initial recommendations for current compliance levels
  - Guidance on checking for current compliance in data logs
    - Did compliance occur during stress and exit compliance after stress
      - Compliance during stress may mask latch-up susceptibility
  - Recommended procedures to follow if current compliance reached
    - Adjusting levels to avoid compliance
    - Determining if reaching compliance was the result of latch-up
    - Guidance of when a valid test can not be done

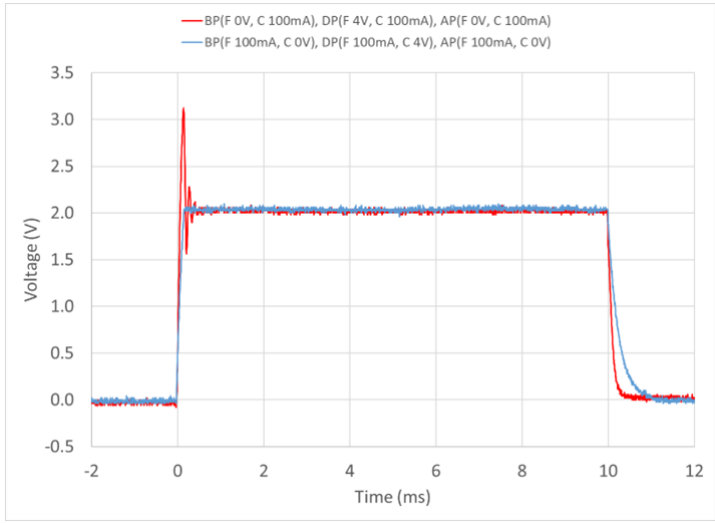
I-Test versus E-Test – Which to Use?

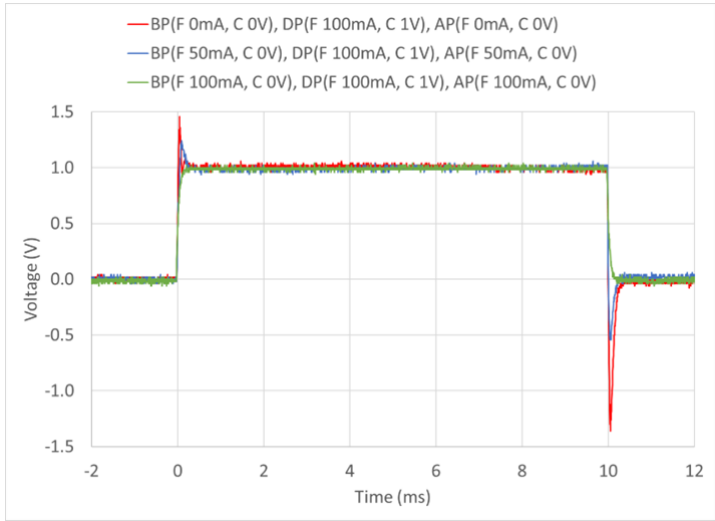
- **Issue**
  - **JESD78F.01 allows Signal pin test with**
    - **I-Test: Current stress with voltage compliance or**
    - **E-Test: Voltage stress with current compliance**
  - **In principle they are the same, in practice they are not**
  - **Which to use?**
    - **Incorrect choice can lead to unexpected stress**

- **User Guide Coverage**
  - **Situations in which reaching compliance results in stress overshoots**
  - **Signal pin types**
    - **Some better with I-Test**
    - **Some better with E-Test**

Waveform Measurements

- **Issues**
  - Are waveforms in specification?
  - Are there pulse source anomalies?
  - Evaluating issues during product testing
- **User Guide Coverage**
  - Measurement setup
  - Oscilloscope specifications
  - Voltage and current probes
  - Measurement system verification
  - Test setup for latch-up pulse source verification
  - When is voltage measurement sufficient
    - Current measurement not always needed
  - How to measure waveforms on product





Pulse Source Measurement Calibration

- **Issue:**
  - **Measurements of the latch-up pulse source may need to be made which can be difficult.**
    - **How are measurements made?**
    - **Do these measurements lead to system calibration?**
- **User Guide Coverage (ref: JESD78F.01, Annex F.01):**
  - **When test results or when test conditions need to be verified:**
    - **Oscilloscope measurements may be the only means of verification.**
  - **The measurements discussed in Annex F.01, show possible anomalies that can occur under certain test conditions.**
    - **Discuss the use of different loads as a means of possibly matching the load of your device.**
    - **Discuss manual test methods which make it easier to setup and capture waveforms.**
    - **System calibration may need certain load conditions for increased understanding**

Pre & Post Voltage/Current Bias/Clamp Levels on Pulse Supply

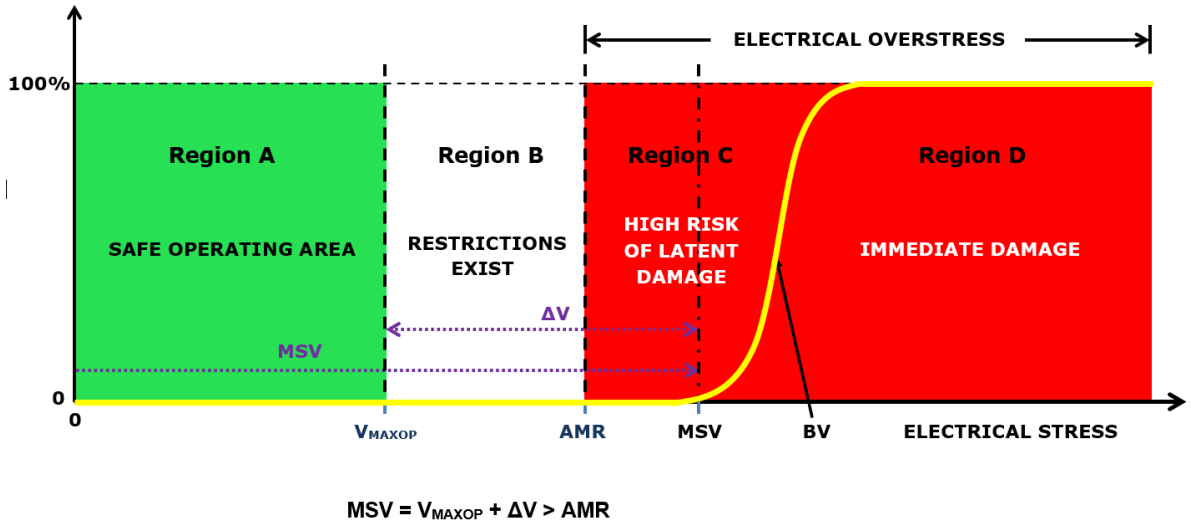
- **Issue: How to set the correct value?**
  - **Are default values always acceptable?**
  - **What values are the best?**
  - **Is there a difference between I-Test and E-Test**

- **User Guide coverage:**
  - **Describe how Pre & Post biases work**
  - **Describe how Pre & Post clamps work**
  - **How these settings can affect stress outcome?**

Maximum Stress Voltage (MSV)

Key Issue: How to Determine MSV for your product pin(s)

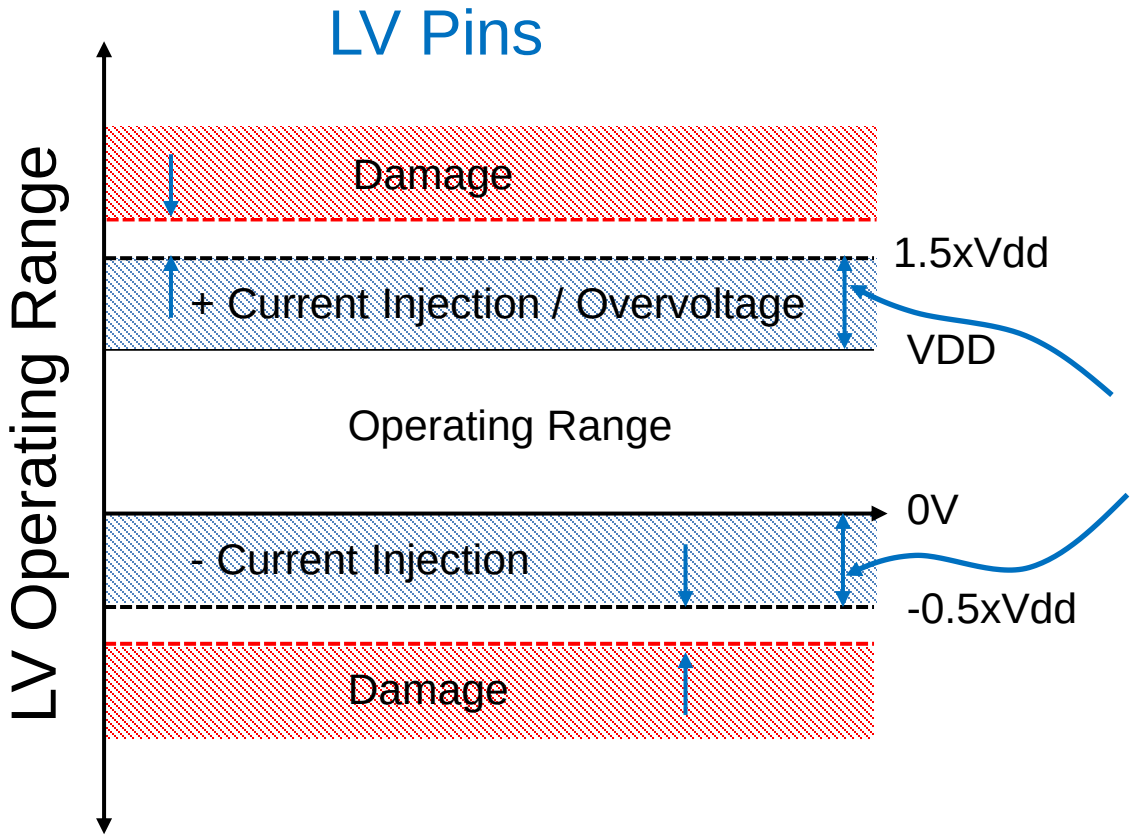
- **What Does User Guide Offer**
  - An Introduction to MSV
  - How to determine MSV in several cases
  - Why MSV is not AMR



- MSV is the Maximum allowable Stress Voltage or Current limit during LU stress that prevents all non-LU reliability failure mechanisms from initiating latent damage during stress

Maximum Stress Voltage (MSV)

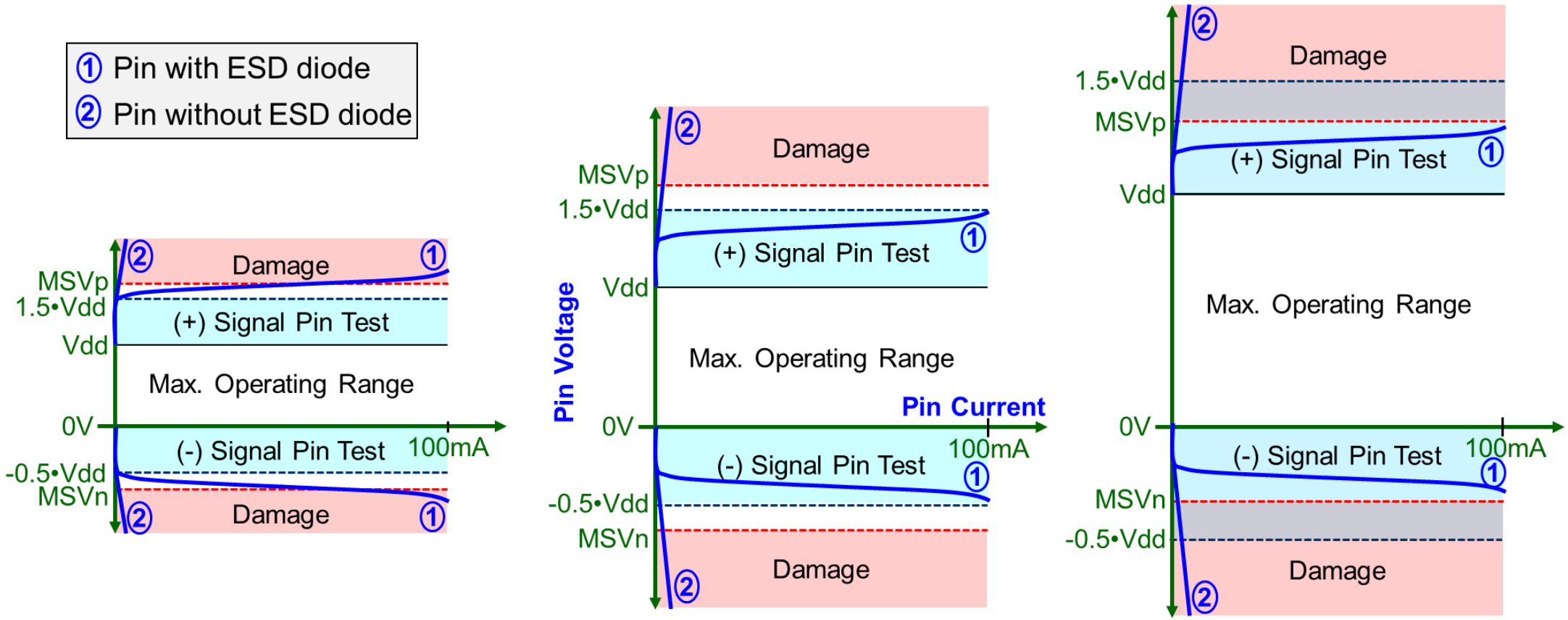
Key Issue: 1.5xV_{maxOP} and -0.5xV_{maxOP} voltage limits only work for some voltage ranges.



Ideal Situation:

- **IOs with ESD diodes: current is injected before reaching V limit**
- **IOs without ESD diodes: V limit reached without damage**

Voltage Range Comparison – LV, MV, HV



LV Pins

(1)✓ **but no current injected**

(2)✓

MV Pins

(1)✓

(2)✓

HV Pins

(1)✓

(2)✓ **but need to invoke MSV**

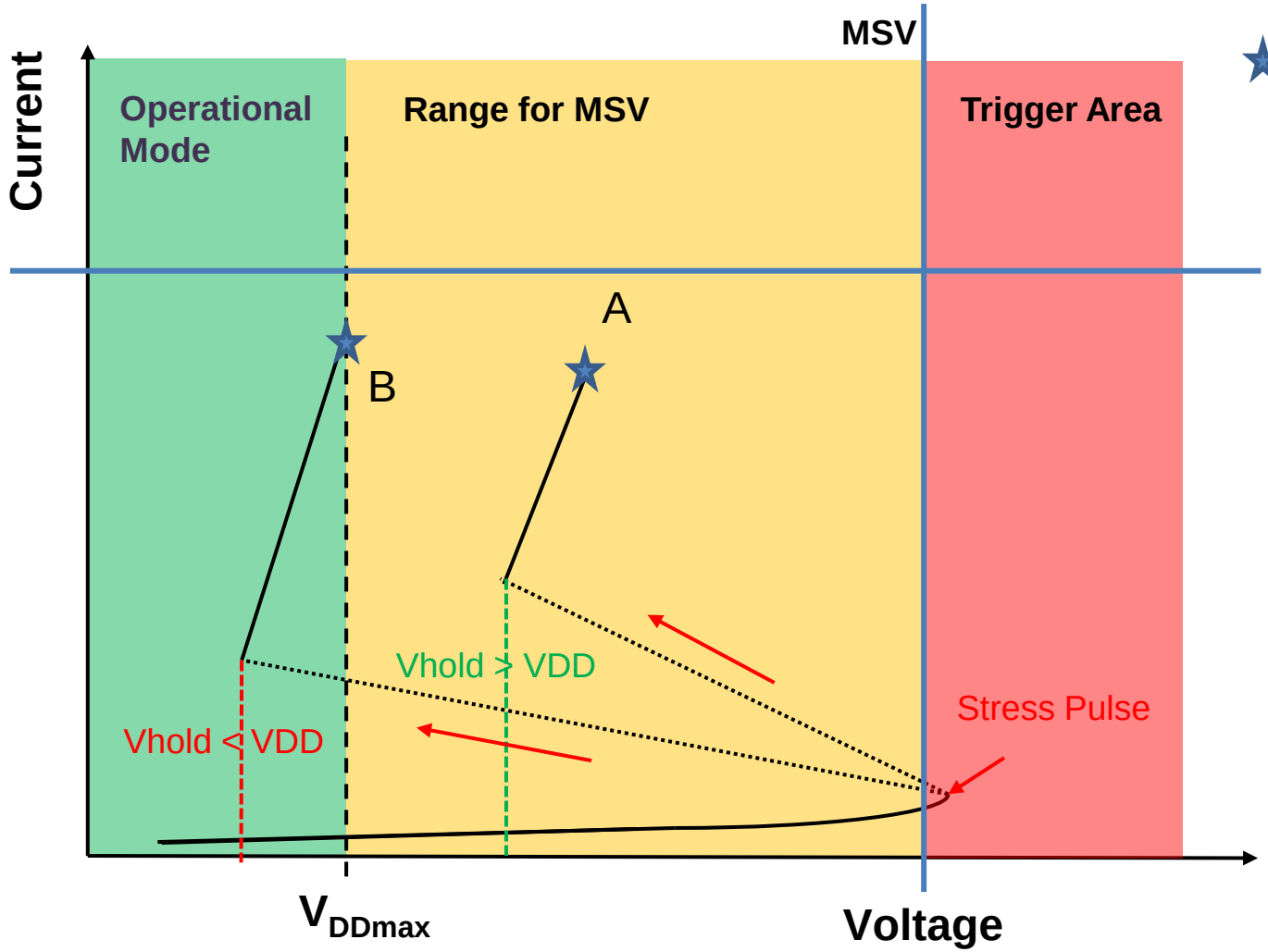
Usage of MSV at Power Clamps

- **Issue:**
  - **Usage of MSV in previous versions allowed reduction of Stress Voltage upon physical damage for HV**
  - **In JESD78F.01 Latchup definition was extended beyond Triggering of Thyristor structures to Power Clamps**
  - **Now: Possible uncertainties arise regarding usage of MSV for HV Power Clamps if physical damage occurs at HV Clamps at Stress Voltages < 1.5 x V_{maxOP}**

- **Approach in User Guide Document:**
  - **Clear guidance for usage of MSV provided:**
    - **It is allowed to invoke MSV also for Power Clamps.**
    - **Condition: Holding Voltage of Snapback >> Vsupply**

Latches in Power Clamps

Triggering of Power Clamp by Stress Pulse



★ **Thermal Destruction Point for both cases**

Electrical Stress Pulse triggers **Power Clamp**; both cases end in thermal destruction

Current Limit for Supply Stress

Case A: Vhold > VDD

No sustaining Latch possible, but thermal destruction ➡ **MSV can be applied**

Case B: Vhold < VDD

Sustaining Latch, thermal destruction

➡ **No invocation of MSV allowed!**

Hardware for Testing of HV products

- **Issue:**
  - **More Products in Automotive and Industrial Applications have Pin Voltages $V_{maxOP} \geq 100V$**
  - **Commercial Testers: No solution available**
  - **Products with Pin Voltage Classes >100V --- unable to be tested on commercial hardware**
- **Approach in User Guide Document:**
  - **Test Hardware**
    - **Specifications for self assembled or modified test solutions must be provided**
    - **Pins must not be defined as "not stressed" or put to GND**
    - **Describe work around solutions possible with actual test hardware**
  - **Test Procedure:**
    - **Preferred solution: To be stressed with V_{maxOP} of Test System (100V)**
    - **Pins with V_{maxOP} > 100V, which were stressed at lower Voltages than specified according to datasheet, must be reported**

Testing of SOI, GaN and other products

- **Issue:**
  - **It is a common assumption that Latchup cannot occur in products of given technologies like SOI, GaN, other compound semiconductors**
  - **Tests are skipped without deeper understanding of the technology**

- **Approach in User Guide:**
  - **Clear guidance must be provided for SOI or non-Si technologies, e.g.**
    - ***JESD78 Test will determine possible allowed technologies to skip testing:***
      - ***WBG Semiconductors (Eg > 1.5eV)***
      - ***SOI Technologies with Thickness of active Si layer < 1 µm***
      - ***Fully/ Partially depleted SOI: PW/NW implants in bulk Si***
      - ***Hybrid SOI/Bulk***

Data Review & Analysis

- **Issue: Monitoring & Analyzing Data**
  - **Supply Collapse**
  - **Injected Currents**
  - **Pre & Post Stress Pulse Bias Currents**
  - **Testing Order**
  - **State Change**
- **User Guide coverage:**
  - **How to analyze data**
  - **Detection of possible invalids and/or failures**
  - **What it means**
    - **Need to adjust clamps**
    - **Adjust the pin set-up**
    - **Need to re-run stress until no invalids and/or failures**

Destructive vs. Non-Destructive Latch-up

- **Issue – Latch-up events can be destructive or non-destructive**
  - **If the silicon substrate and interconnect associated with the latch-up event can sustain the current flow and**
  - **Without damage until the latch-up event is terminated**
- **User Guide Coverage: Discuss Methods of Assessment**
  - **Destructive latch-up – factors affecting susceptibility to damage**
  - **Non-destructive vs destructive latch-up – post stress evaluation**

The JESD78 workgroup is waiting for you to join!