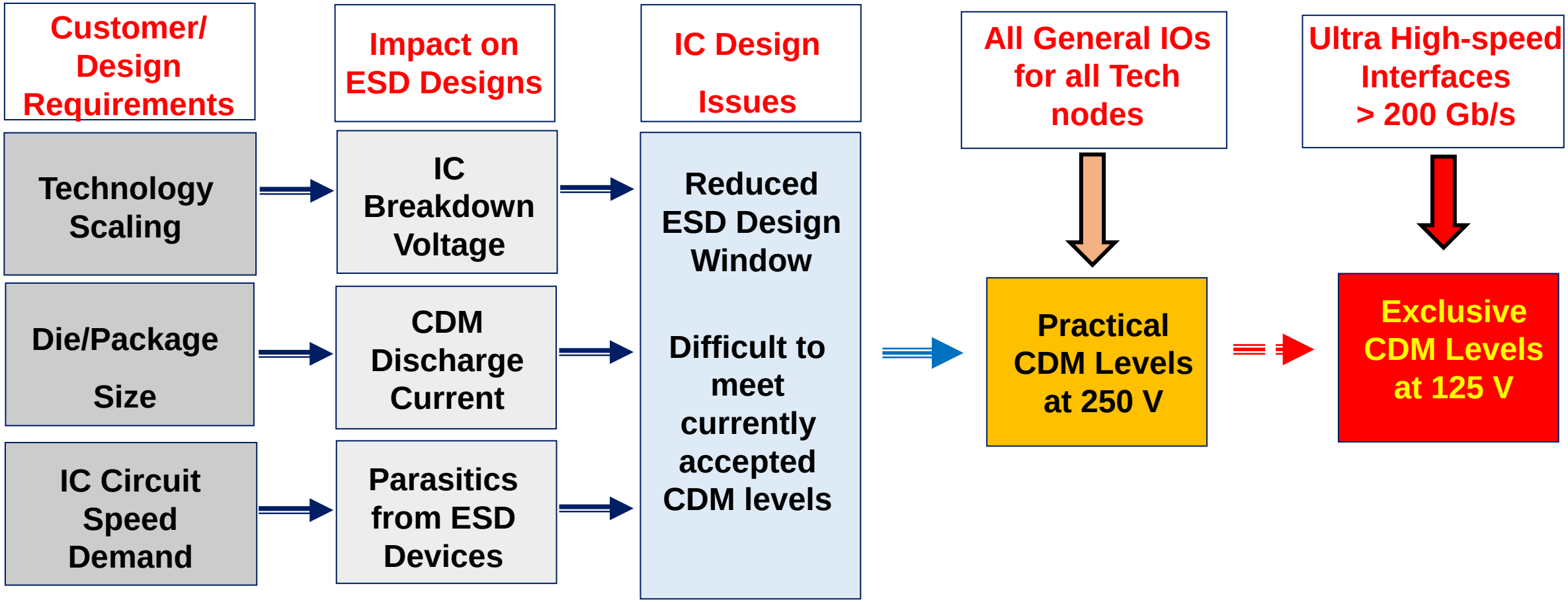
Industry Council on ESD Target Levels

Evaluation of CDM Targets

In A Nutshell

- Since its first publication in 2009, JEP157 on CDM Target Levels has been a very popular and important reference to the industry for CDM ESD qualification
- While all the technical information is still valid, perspectives have changed with special reference to advanced technologies for ultra high-speed applications
- As such, this new revision focuses on relevant information that is up to date and details a better target level roadmap to meet these new applications
- The document revision also adds new information on CDM qualification testing alignment and issues related to external IP interfaces
- Addresses projected 3D IC CDM targets for the first time
- While most of the document is intact it should be noted that some of the modifications required updating some of the original figures to be commensurate with the overall new message – old figures were replaced with more inclusive information dealing with newer technologies

Overview: CDM Technology & Design Issues



Exec Summary

- IC design constraints make it increasingly difficult to meet the current CDM levels as technologies continue to shrink and the circuit speed demands continue to increase
- Previous WP showed that devices with CDM levels below the general target of 500 V could safely be handled with CDM control methods available in the industry at the time
  - Based on these observations and constraints it was established that 250 V was a safe and practical target CDM level in general (≤ 56 Gb/s)
- The work in this extension addresses the issues for high-speed interface designs (>56 Gb/s) where this 250 V level cannot still be met – ultimately reaching ultra-high speed interfaces >200 Gb/s at 125 V
- Handling of these high-speed interface pins, that could force CDM target levels below 200 V, requires more comprehensive process assessments in manufacturing
- Finally, die-to-die interfaces (2.5D and 3D ICs) require a special CDM roadmap that is also outlined in this work.

Outline

- Relevance of CDM
- CDM Technology & Design Issues
  - ESD Design window
  - Package size
  - Limitation in capacitive load
- CDM Qualification Methods
- ESD Control Methods Addressing CDM
- Die-to-die Interface CDM Roadmap
- CDM Peak Current Qualification for IP
- Conclusion

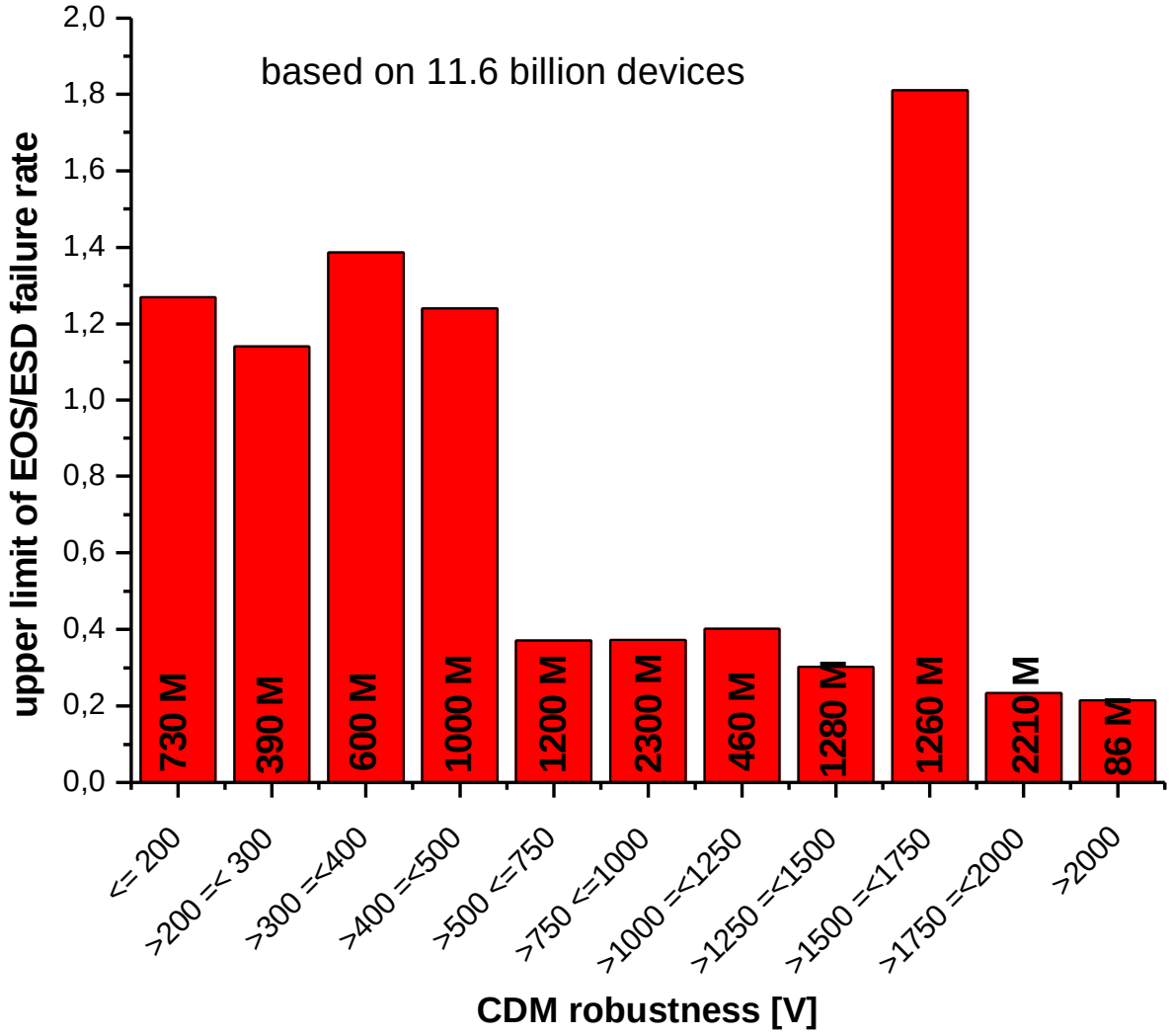
Relevance of CDM

- CDM is a unique and important test method for IC component ESD testing
- There are proven damage signatures of field returns due to fast ESD discharges with high peak current that cannot be reproduced by HBM
- CDM testing can effectively replicate these failure signatures
- Typical discharge scenarios are known in IC testing and manufacturing which cause CDM failure signatures
- **➔CDM is a necessary and important qualification test**

Analysis of FAR Data

- FAR data was collected from various Council members on over 11 billion shipped IC's.
- Field returns include returns from handling and testing at IC supplier, manufacturing of the PCB and the end-customer returns.
- 949 designs have been included covering automotive, consumer, memory and discrete products.
- The presented data were collected in the time frame from 2003 to 2007.

Field Return Data versus CDM voltage



- Important Observations:
  - EOS/ESD failure rates do not show a clear trend in dependence of the CDM voltage
  - A few designs with high return rates (outliers) dominate the statistics

Further Limitations:

- **Device not always tested to failure voltage**
- **Discrepancy between JEDEC and ESDA tester**
- **Rel. Humidity during testing not controlled/recorded**

Conclusions from FAR Data Analysis

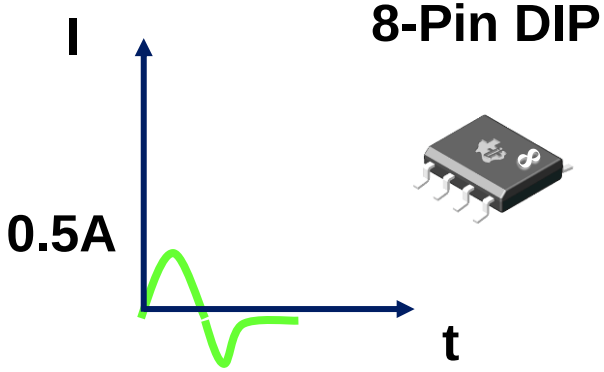
- EOS/ESD FARs can appear for any level of CDM from <200 V to >2000 V
- FARs with clear CDM damage can be seen for ICs with very low CDM passing level
- Proven CDM-type events occasionally occur during the ramp-up phase of a new handling/testing process at the IC supplier.
- FARs during ramp-up can also occur for devices with greater than 500 V CDM robustness.
- Addressing the failure mechanism by proper ESD control measures solves the problem. Usually only a minor effort combined with a low investment in cost is required.

CDM field fails can occasionally occur with significant return rates during ramp-up. This must be solved by ESD control measures.

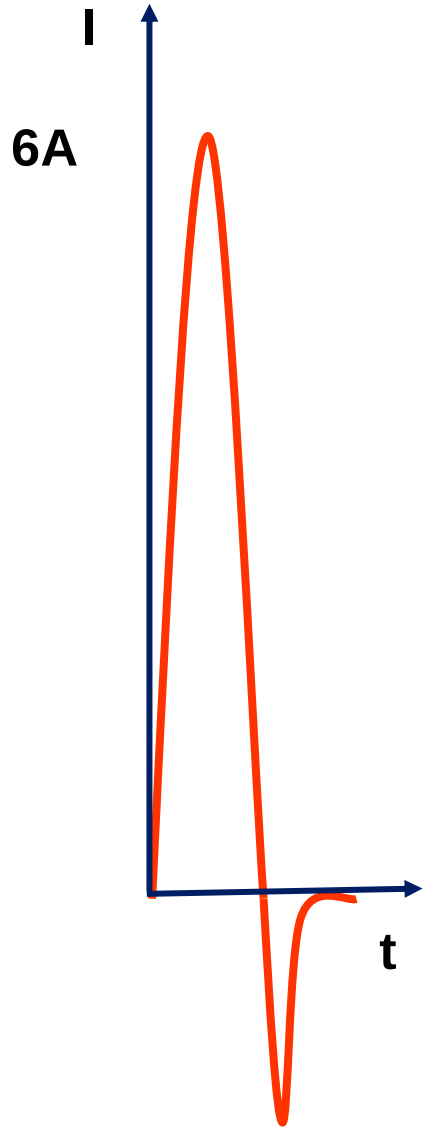
CDM Technology & Design Issues

- CDM protection design is primarily driven by the peak current from the IC package discharge at the required (targeted) CDM voltage level.
- Increasing package size (increasing capacitance) leads to increased CDM peak current for a given CDM stress voltage.
- CDM protection adds capacitive and resistive parasitics to high-speed interfaces, and these parasitics can have an impact on higher operating frequencies.
  - This sets limits on ESD protection device sizes and therefore ESD robustness
- Additionally, CDM protection design is increasingly limited by reduction in breakdown voltage of gate dielectrics and junctions.
  - CDM protection design requirements at a few Amps of peak current can create a severe limitation for present high-speed interface designs.

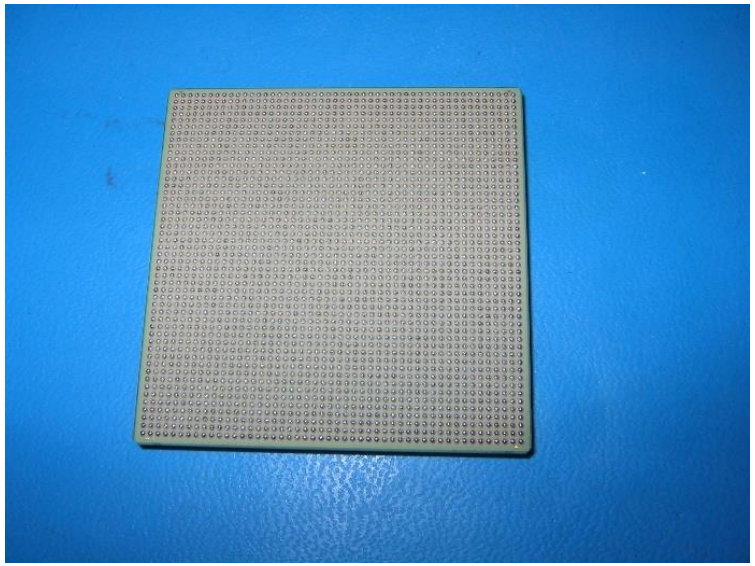
Impact of Package on CDM Discharge Current @250 V



8-Pin DIP

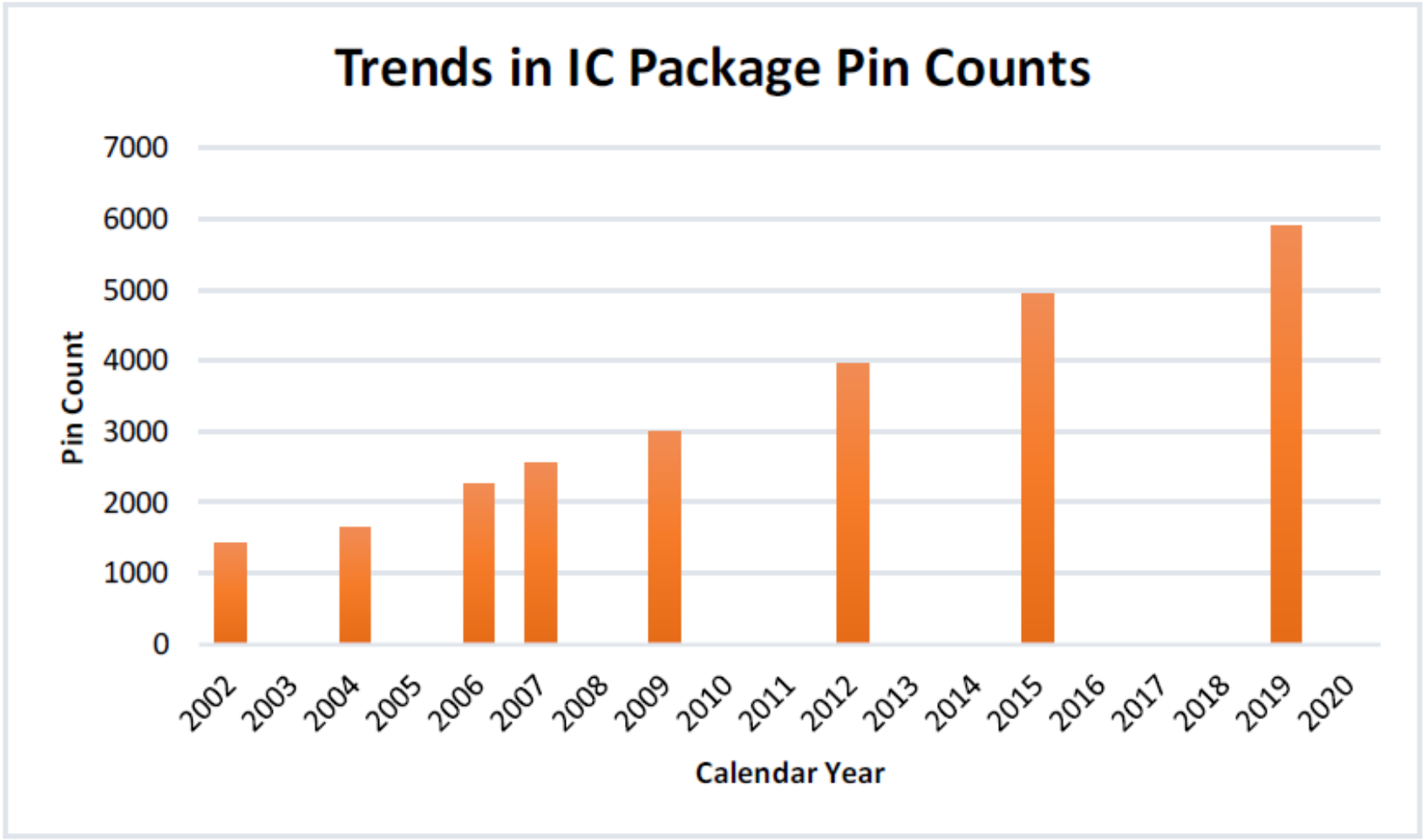


2400-Pin LGA



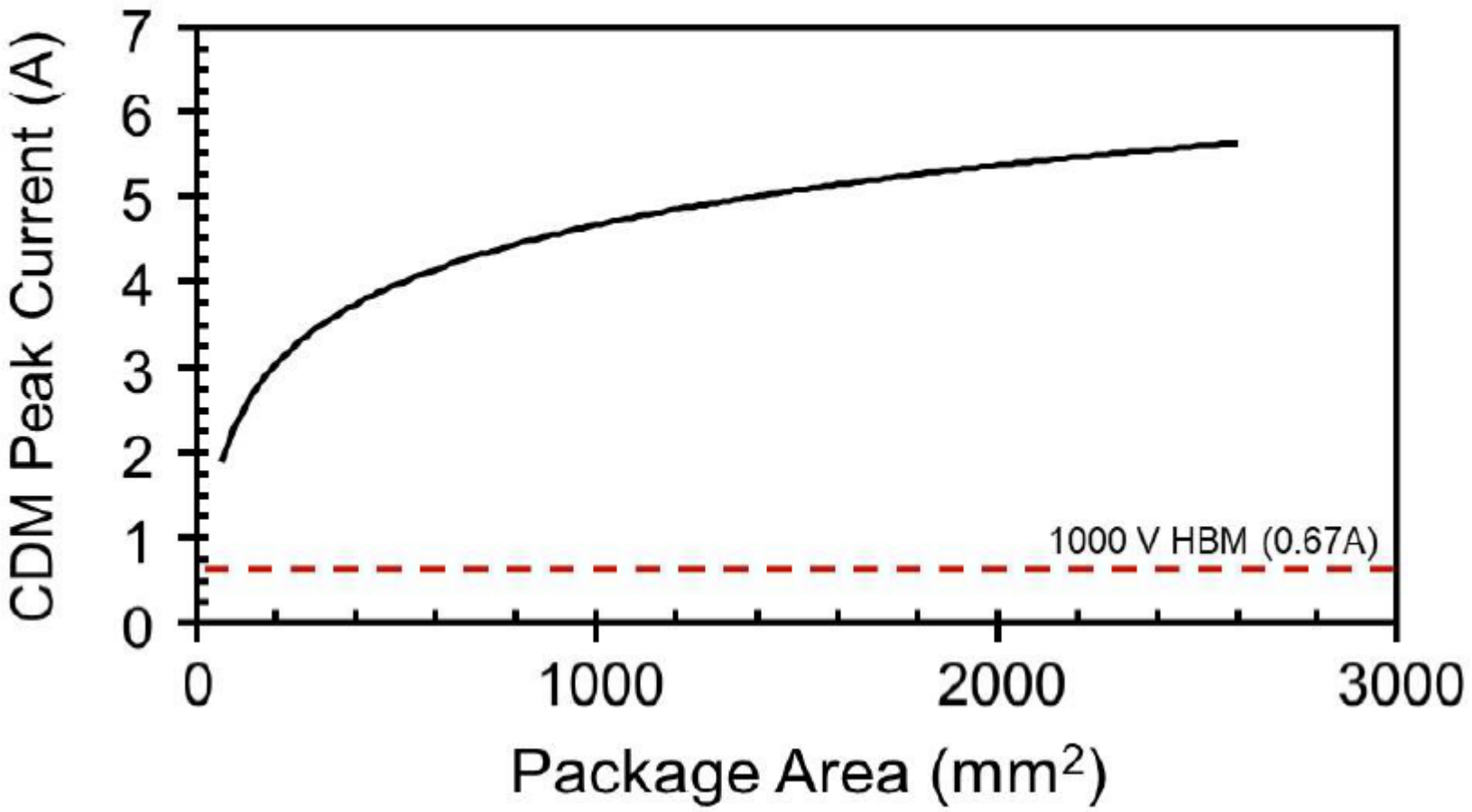
Wide variations (15X) in the peak discharge current from the smallest to the largest IC packages

Trends in IC Package Size



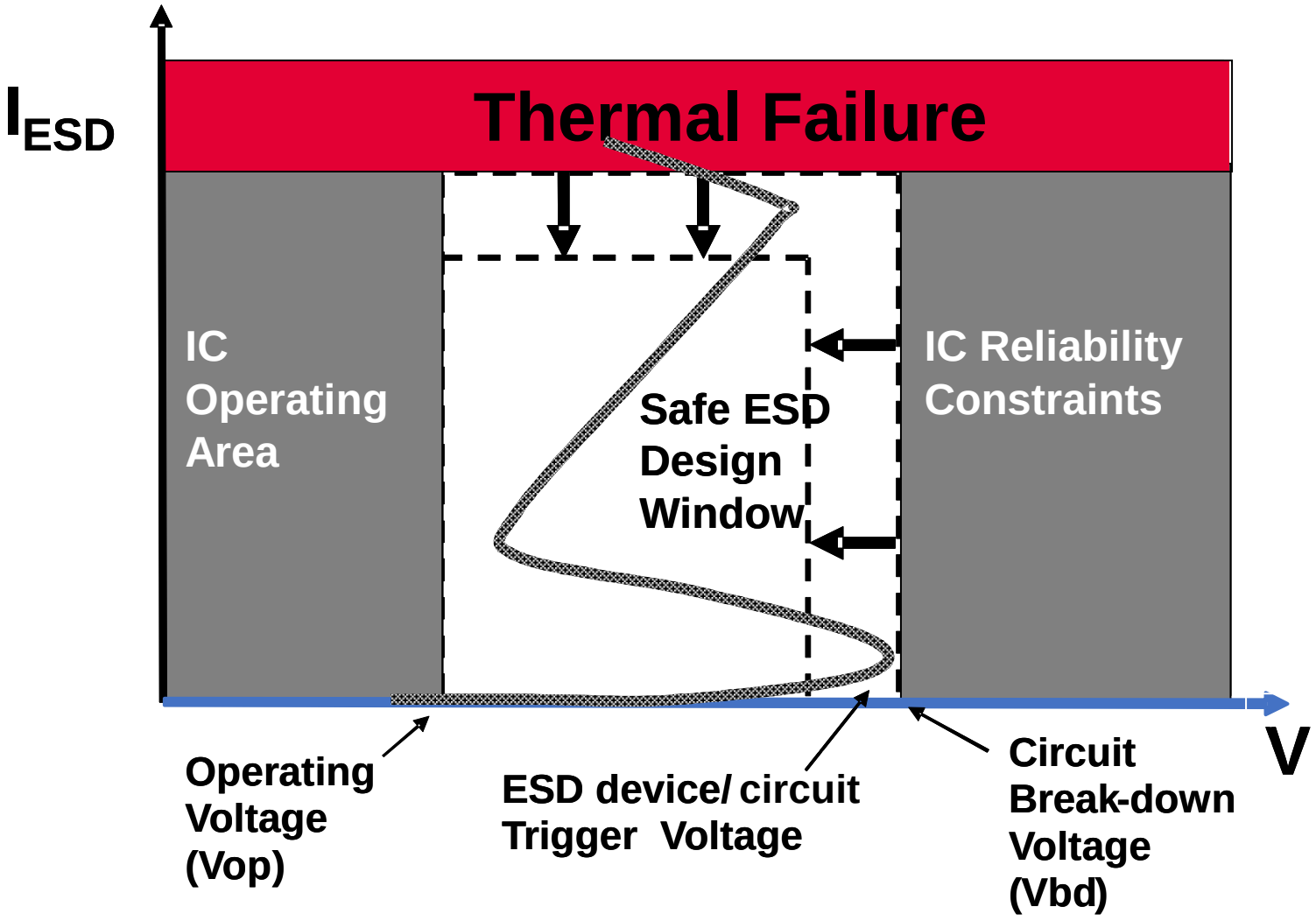
- Higher pin count devices at every new tech node are market driven by high performance pins on microprocessors

Consequence for Typical CDM Peak Current at 250V



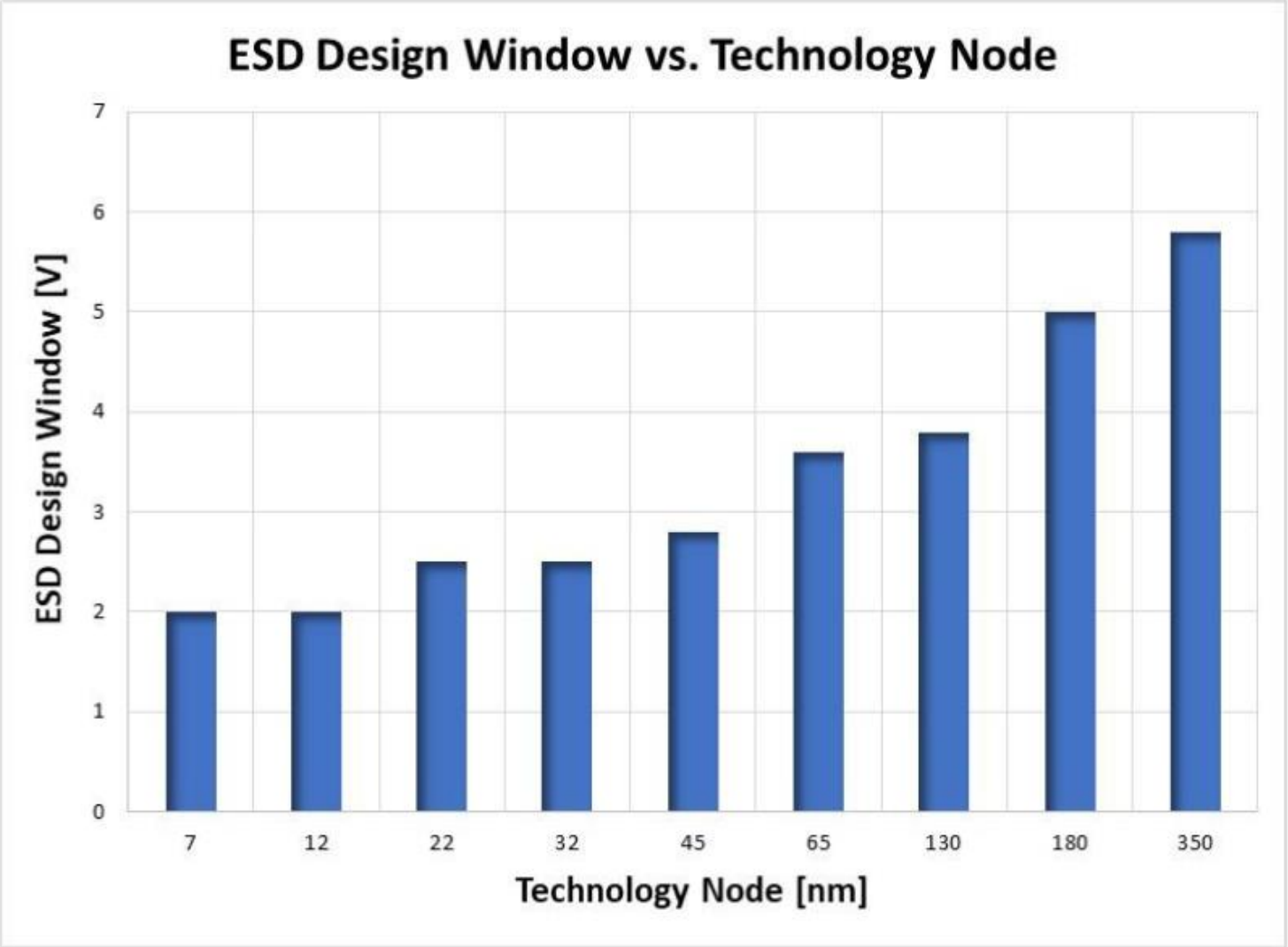
- CDM peak current increases with increasing pin count/package area

Impact of Downscaling of Technology



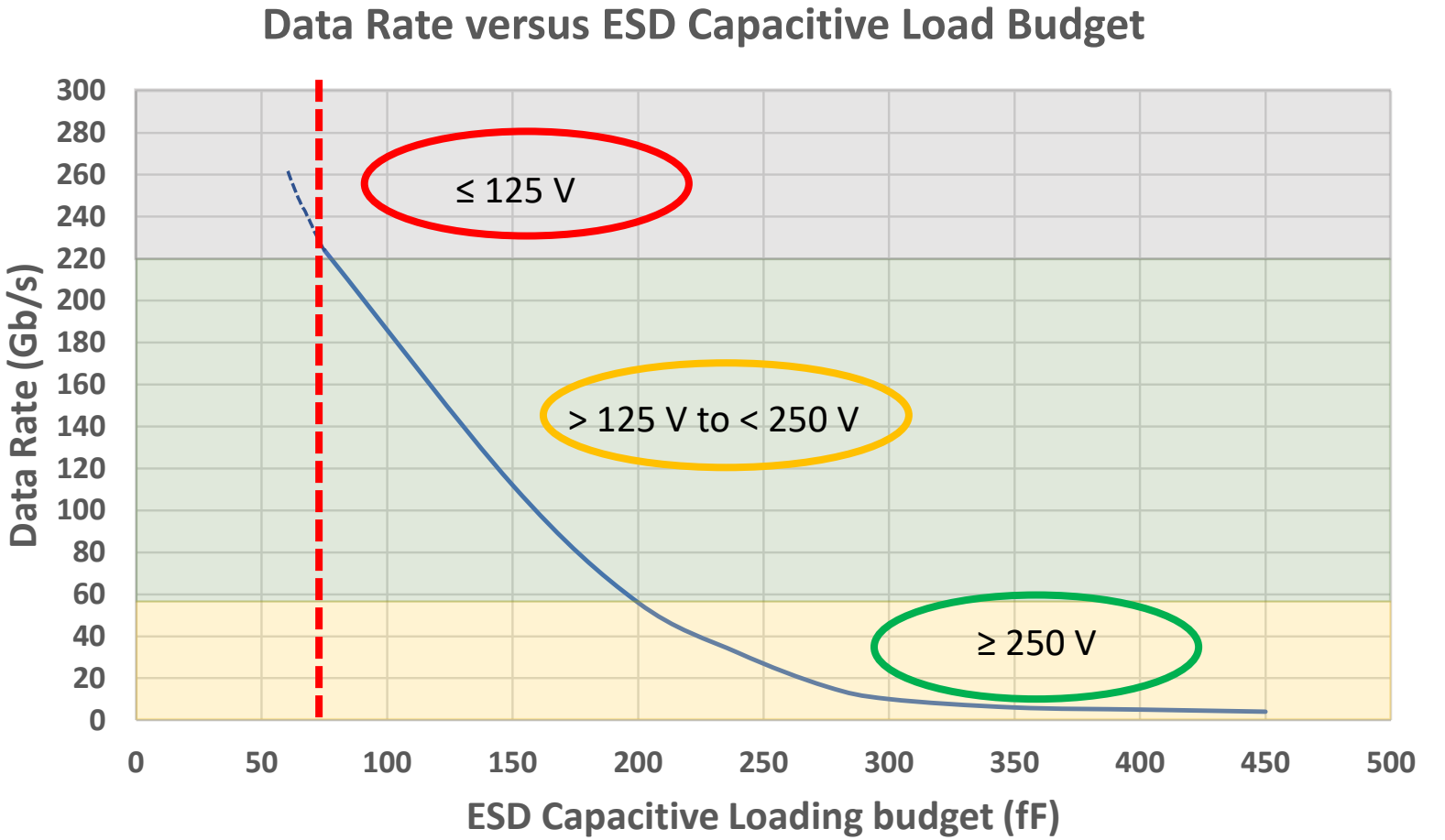
- Downscaling of gate dielectrics lead to a shrink in the available voltage window
- Decrease in device size limits the maximum current density before thermal fail occurs

Limitation of CDM Protection Design Due to Gate Oxide Shrink



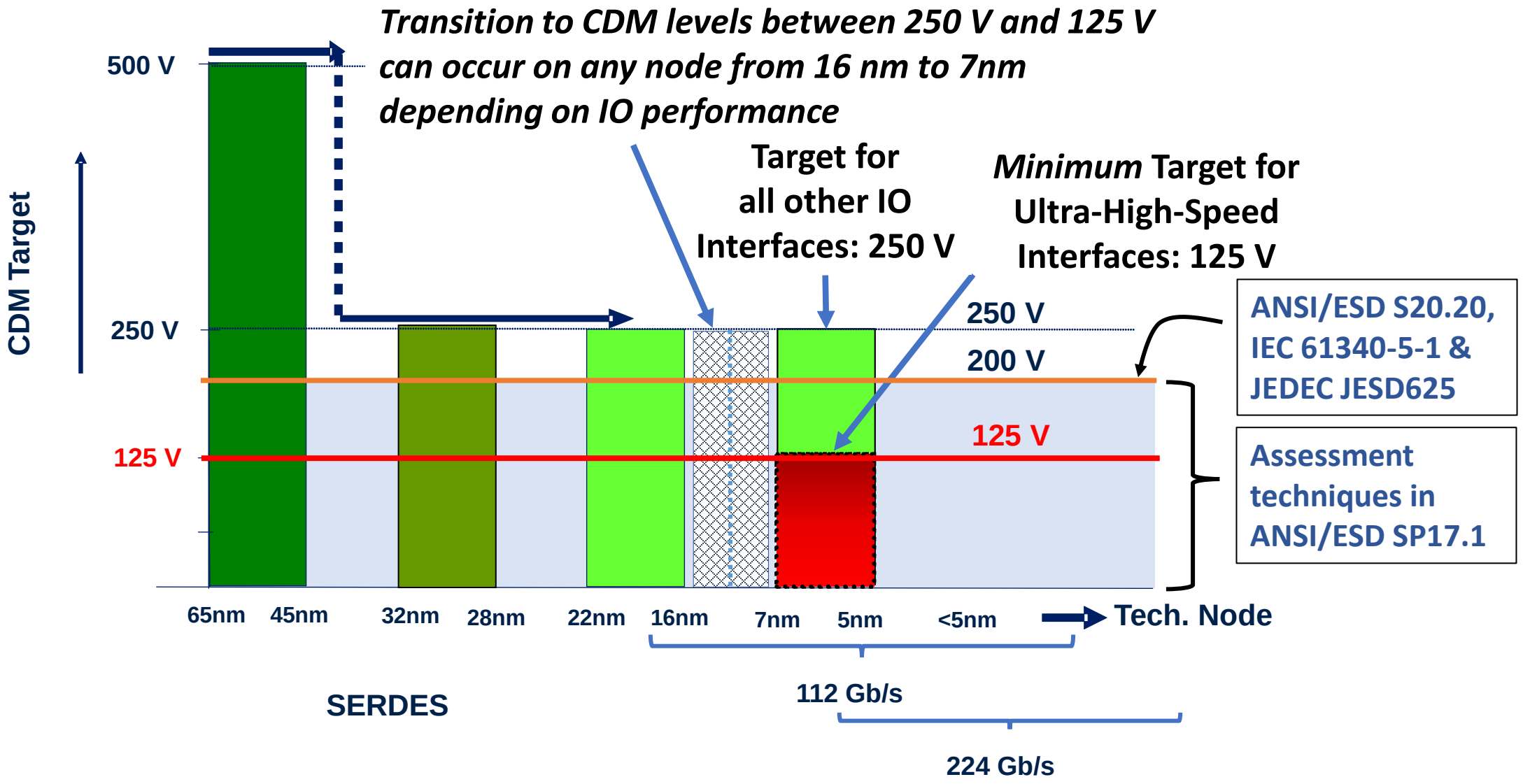
- Most critical for CDM is the downscaling of the dielectric breakdown voltage.
- This has reached a critical value for thin gate oxide < 1.5 nm, which is typical for 65 nm and below.
- There is no significant relief seen when gate oxide is replaced by high-K materials.

Capacitive Effects of Data Rates vs. CDM Levels



- For ultra-high-speed IO at 224 Gb/s, the ESD capacitance loading is limited to < 75 fF
- CDM voltage decreases for higher data rate designs due to:
  - smaller diode sizes
  - lower oxide breakdown voltages
- Forcing CDM designs down towards 125 V

New CDM Qualification Roadmap



Conclusions from Protection Design Constraints

- The following industry/technology trends are seen:
  - Increasing IC package capacitance (from larger package sizes) results in increased CDM peak current for a given CDM stress voltage
  - Higher operating frequencies force a reduction in CDM protection parasitics and thus its effectiveness
  - Higher sensitivity of the IC devices due to technology scaling
- These trends have led to an initial white paper recommendation of CDM design protection at a 250 V qualification voltage for mid and high-speed applications.
- For ultra-high-speed a target level of 125 V is recommended, at data rates above 56 Gb/s, depending on package size, 250 V may not be achievable, but target should be maximized to reduce manufacturing risks
  - All other IO should still target 250 V

Recommendation For Ultra High-Speed Interfaces

For ultra-high-speed interfaces operating at 56 GHz (Nyquist) or 224 Gb/s PAM4, where only a CDM target level of 125 V is achievable:

The recommended target peak current for a 224 Gb/s ultra-high-speed IP block is 2.5 A

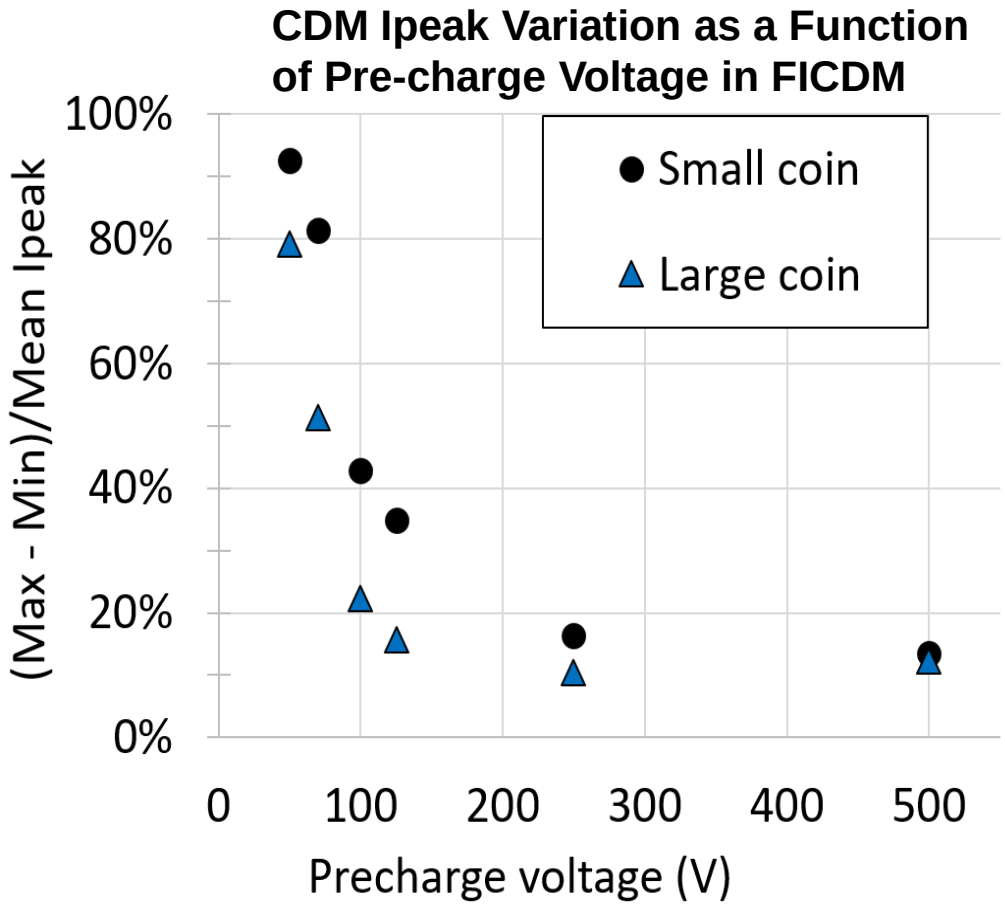
CDM IC Qualification Standards

Standard	Issuing Body	In this document
ANSI/ESDA/JEDEC JS-002-2018 [1]	Joint ESDA & JEDEC	JS-002
EIAJ ED-4701/300-2 Test Method 305 [4]	JEITA	JEITA CDM
AEC - Q100-011 Rev-D [3]	AEC	AEC CDM
IEC 60749-28:2017 [2]	IEC	IEC CDM

- **Four widely** used CDM qualification standards
- However, there are really only **two base standards** :
  - ANSI/ESDA/JEDEC JS-002 (AEC and IEC standards are based on JS-002)
  - JEITA CDM standard

CDM Testing Challenges at Low Voltages

- As target levels are reduced – air spark variation will increase in field-induced CDM testing
- Target levels at 125 V will need a contact-based method to improve reproducibility at these lower levels
- Contact based methods such as Low-Impedance Contact CDM or Capacitive Coupled TLP may be better alternatives

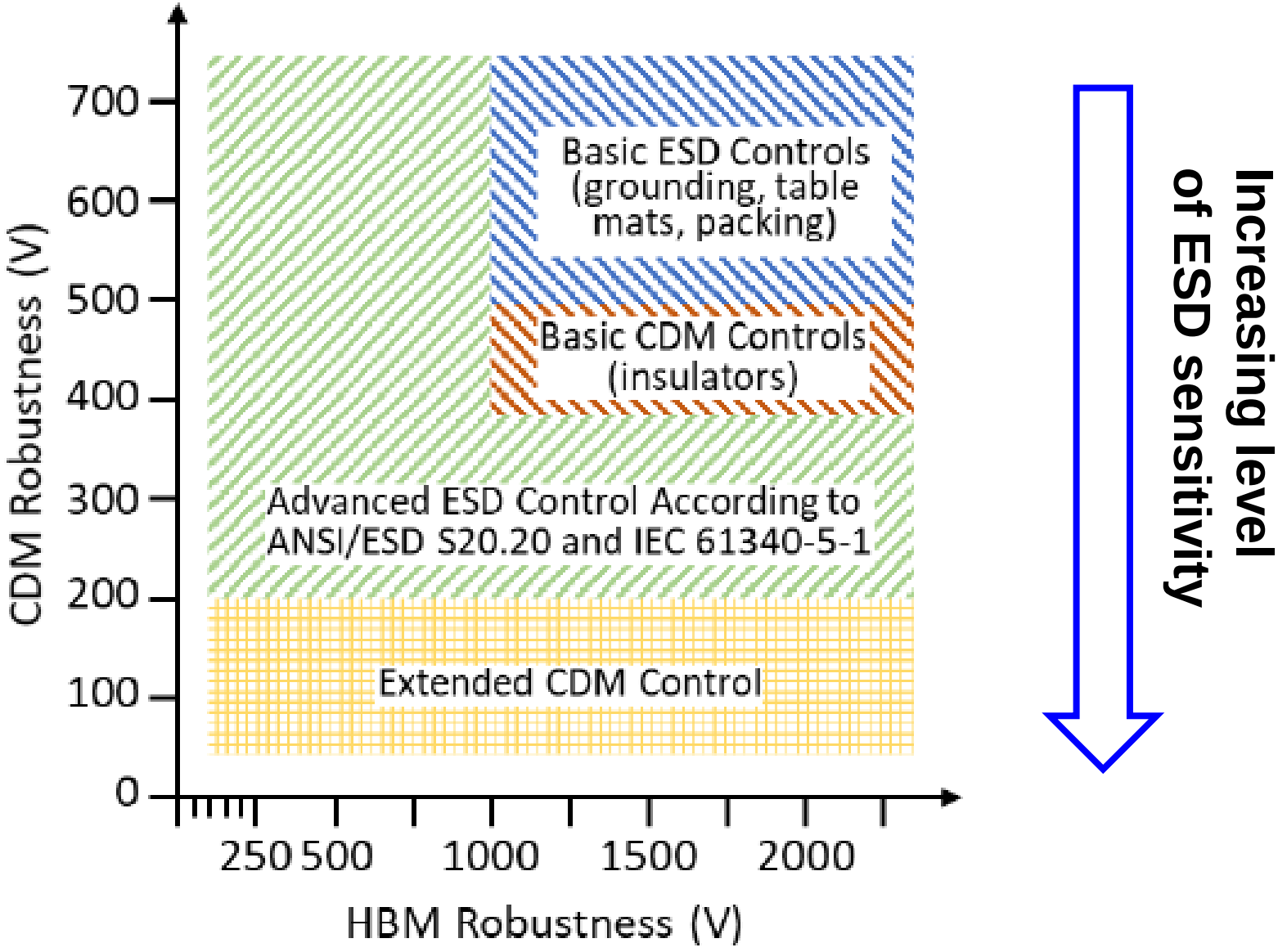


CDM Risk Analysis

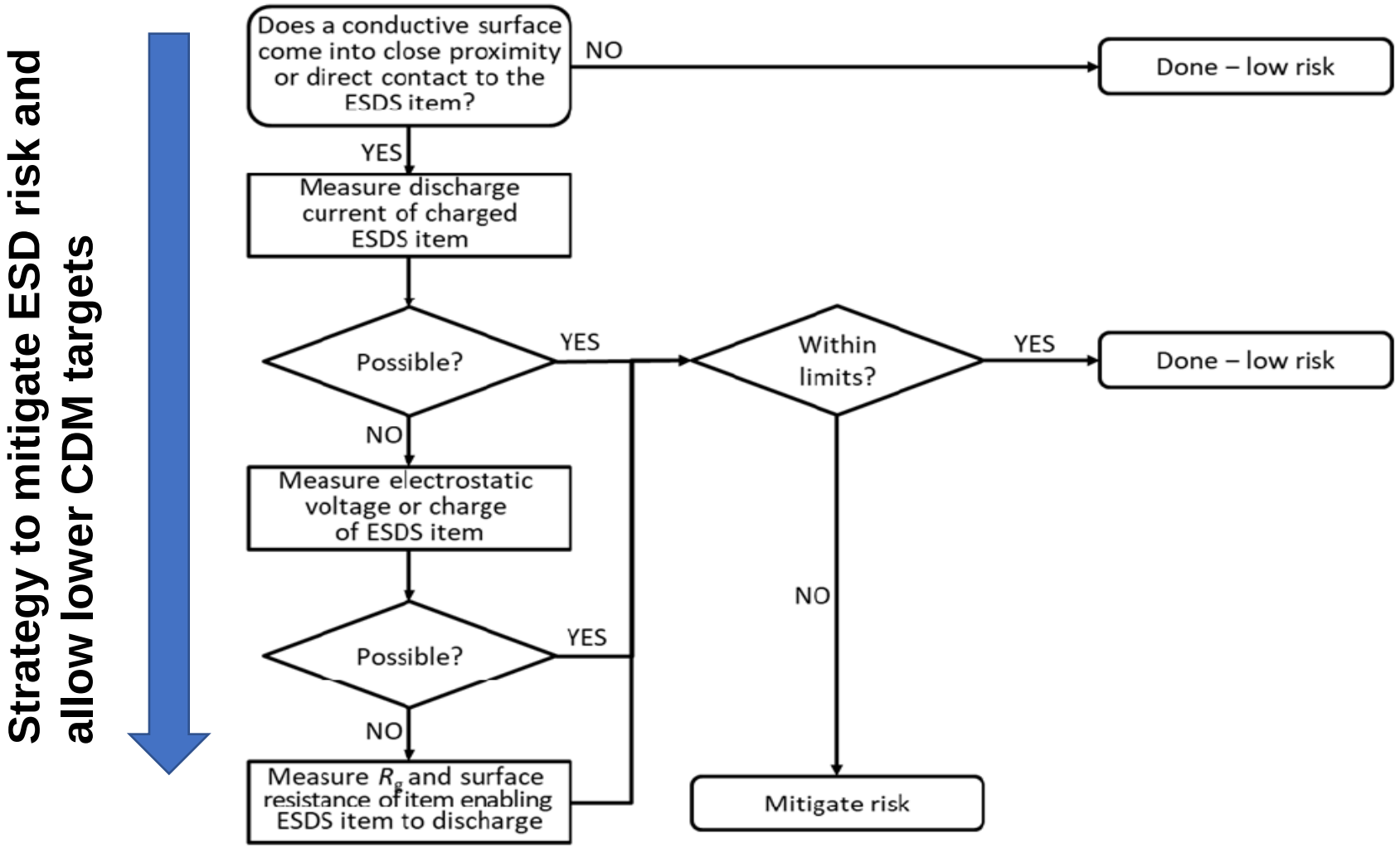
- CDM risk analysis may need to be done more often by
  - Analyzing the E-field in the area where ICs are handled
  - Detection of discharges for process monitoring
- Based on the empirical experience of the ESD control experts the measured values of these measurement methods can be related to a CDM threat level
- Threat levels of devices/PCBs need to be measured and verified at all process steps
- Change of process, change of material, ionization or other charge mitigating techniques may need to be introduced at the critical handling steps

Relationship between General ESD Control and CDM Specific Control

- ANSI/ESD SP17.1 introduces advanced process assessment techniques which can be used to determine risks with lower CDM levels in both manufacturing and field service in the “extended CDM control” region



Flow to Assess the ESD Risk Induced by Charged ESDS Items according to ANSI/ESD SP17.1 (Released January 2021)

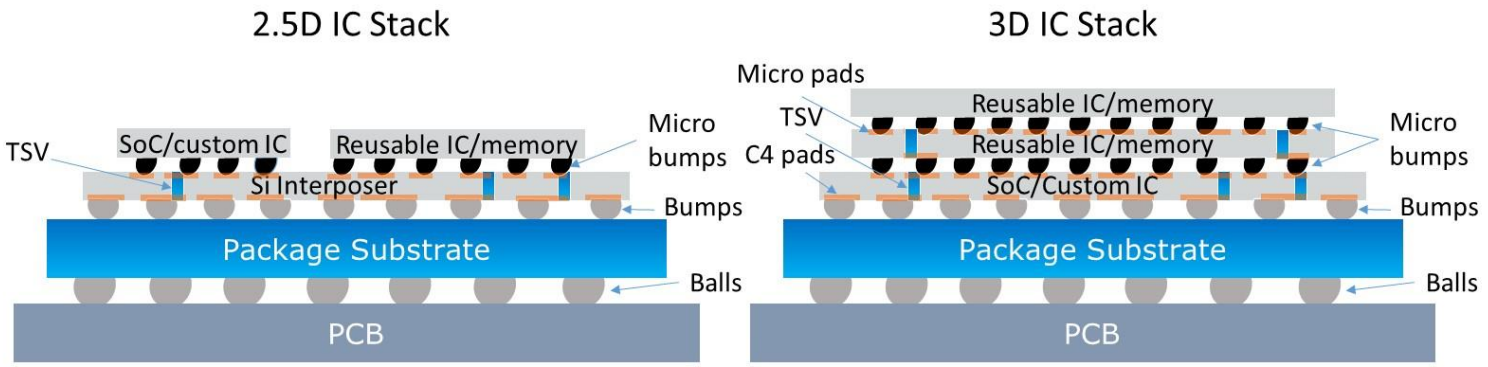


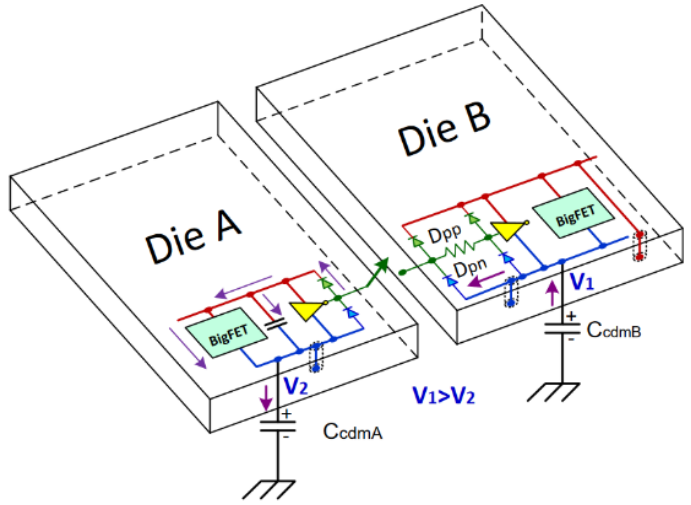
Updated CDM Classification Based on Factory CDM Control

CDM classification level (tested acc. to ANSI/ESDA/JEDEC JS-002)	ESD Control Requirements
$V_{CDM} \geq 200$ V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators according to standards like ANSI/ESD S20.20, IEC 61340-5-1, or JEDEC JESD625
$V_{CDM} < 200$ V	• **Basic ESD control methods** with the grounding of metallic machine parts and control of insulators **+** • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads) **+** • **Charging/discharging measurements at critical process steps following ANSI/ESD SP17.1**

CDM Targets for Die-to-Die Interfaces in 3D IC

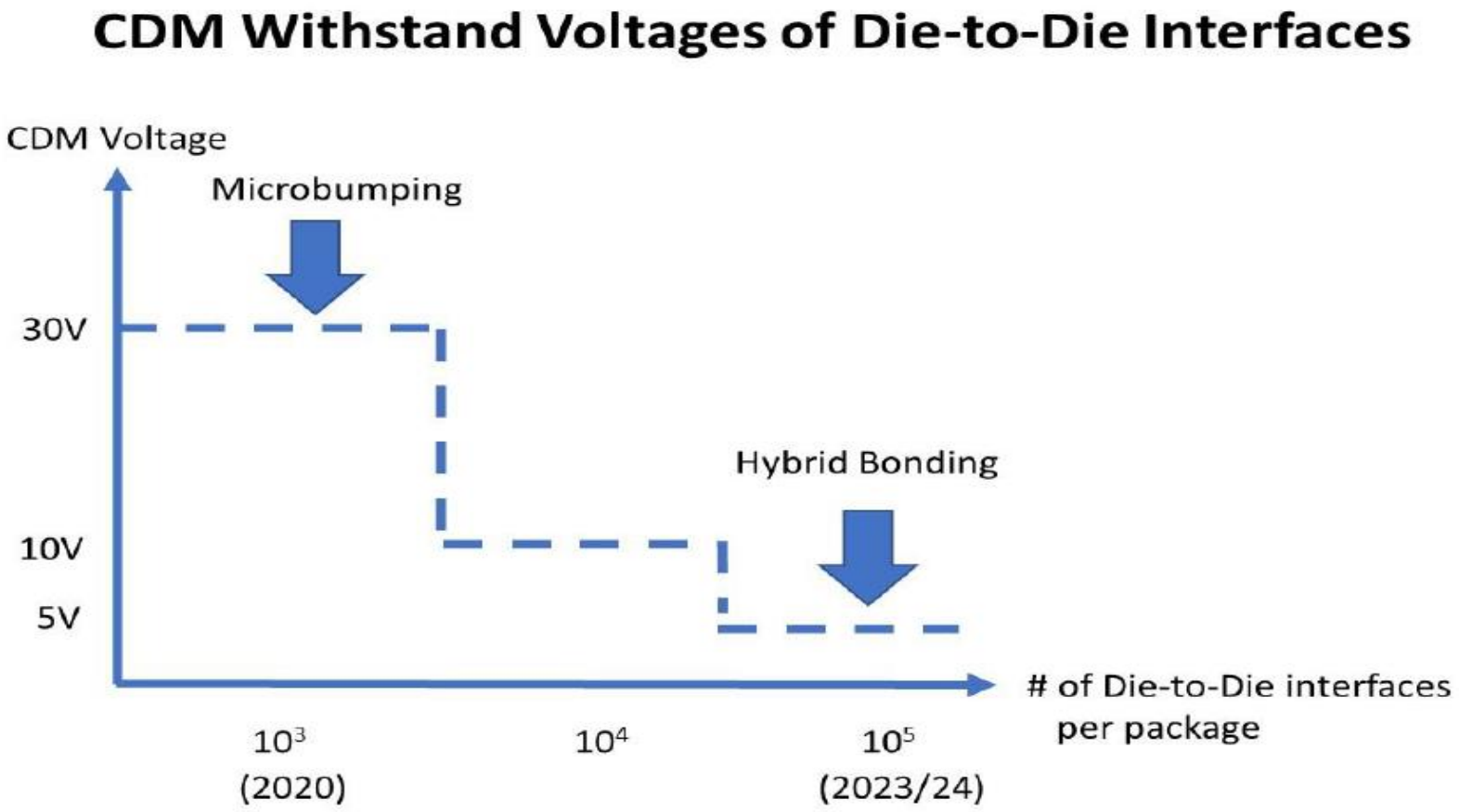
- Refers to description in GSA whitepaper “Electrostatic Discharge (ESD) in 3D-IC Packages” Version 1.0 January 14, 2015
- Careful control of a few critical process steps will guarantee safe handling for a typical target CDM of 35 V (Ipeak between 100 mA to 200 mA for smaller die size < 100 mm^2).
- Due to the high area footprint for high density µbumps or hybrid bonds the target level needs to drop (recommendation of 5 V by 2024)





CDM Targets for Die-to-Die Interfaces in 3D IC

- Recommended to verify the robustness of representative micro-bumps using a VF-TLP pulse setup, wafer level LICCDM, or wafer level CC-TLP instead of full scale CDM qualification. This can also be performed on test chips and be referenced for the final product.

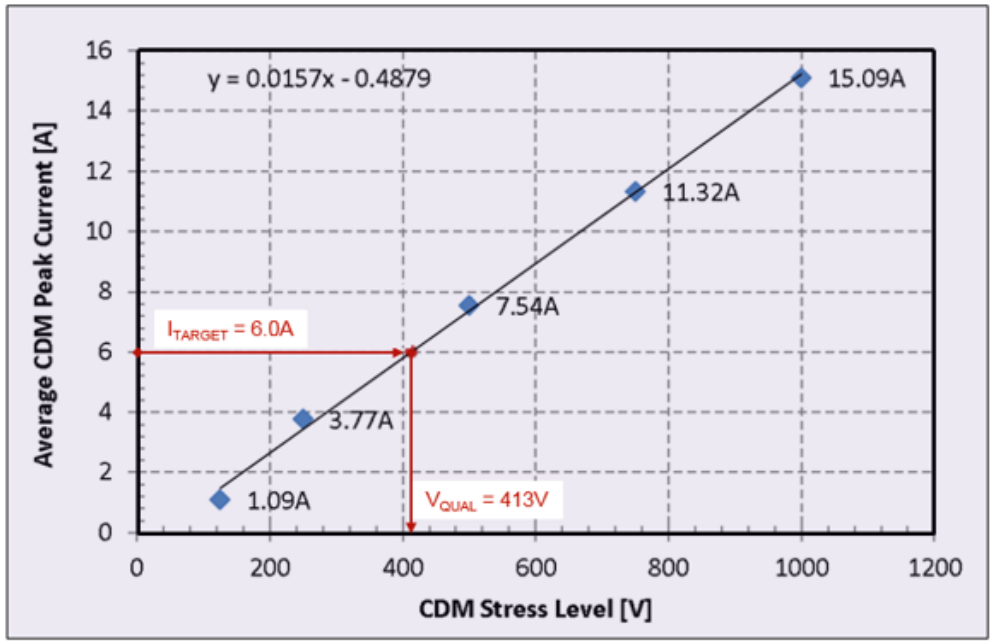


CDM Qualification of Interface IP Requires Special Approach

- CDM *product* qualification is based on voltage classification
  - Purpose: Links the product robustness with discharge threats in factory
- For *pre-validated IP* the CDM voltage classification does not make sense
  - The discharge peak current at given CDM voltage strongly depends on the package and will thus be different on test chip and product
  - Failure is ultimately caused by the peak current regardless of the CDM voltage
- IP passing qualification on test chip may fail same voltage level in product!
- The CDM qualification parameter for IP should be a *peak discharge current* instead of a voltage level
  - The IP will pass similar peak current level in product as on test chip
- Proposal for a CDM qualification method based on peak current on next slide

New Methodology for CDM Qualification of Interface IP

- CDM performance with external IPs is always uncertain and a clear method is needed
- **Step 1**: determine peak current vs. CDM voltage correlation for the test chip
  - Monitor the average peak current at different levels
  - Determine the CDM voltage setting for the targeted peak current
- **Step 2**: execute the actual qualification following the standard procedure, e.g.
  - Use CDM voltage setting from Step 1
  - Stress the pins and apply post-stress test



Example of peak current vs. CDM voltage plot used to determine voltage setting for 6A target

- **Result:** Pre-validated IP for a minimum CDM discharge peak current withstand level

Conclusions

- CDM targets levels are more challenged in the future as the demand for high-speed IO interfaces prevail
  - Lowering the target to 125 V specific to ultra-high-speed applications is necessary to achieve data rates of 224 Gb/s or higher
  - At data rates above 56 Gb/s, depending on package size, 250 V may not be achievable, but target level should be maximized to reduce manufacturing risk
- At such low CDM targets, concerns for test method accuracy and factory control techniques is becoming very important
- Die-to-die interfaces constitute a new critical class of IOs with minimal CDM protection

Supporting Material

External versus Internal I/Os

External and Internal High-Speed Interfaces

- Ultra-high-speed interfaces have limited ESD protection
  - How to detect those I/Os that have higher ESD risk levels?
  - What type of I/Os have a higher probability to be exposed to ESD stress and get damaged during processing, installation, and use
- I/Os can be classified as *Internal* or *External*
- External / internal classification can be used;

  a) to build up ESD protection for manufacturing, handling, and maintenance phases

  b) to optimize external protection by using on-board circuits or by shielding the interface

  c) to ensure passing IC, module, or system level qualification tests

External and Internal High-Speed Interfaces

- Exposed high-speed I/Os in the end product
  - Can have on-board ESD protection and RF filters along the signal net
  - Can be well protected against ESD stress
  - Can have limited or non-existing on-chip and on-board protection
  - Can be well protected after a data cable has been connected
  - Cable discharge event risk exists during installation / maintenance

- Product internal high-speed I/Os
  - Typically used to connect sub-assemblies or PCBs together
    - Can have relaxed ESD requirements → ESD sensitive
  - Can be contacted during IC manufacturing, testing, and tuning
  - Interfaces can be contacted during system testing and tuning phases
  - A charged IC, connector or PCB can initiate a charged device event during part assembly

Visible or Accessible External I/Os

- Decreased risk when:
  - There is onboard protection between the I/O and the exposed interface
  - Signal net is inside the PCB and the interface has a shielded connector
  - The interface is connected to an optical module and the module is shielded

- Higher risks when:
  - There are limited or no onboard protection components between the I/O and the exposed interface. The interface can be contacted by the end user
  - The signal net is tested or contacted during frontend, backend, or PCB assembly phase
  - Connectors, ICs or PCBs can have static charges during assembly or testing
  - A high number of high-speed I/Os on each PCB or sub-assembly

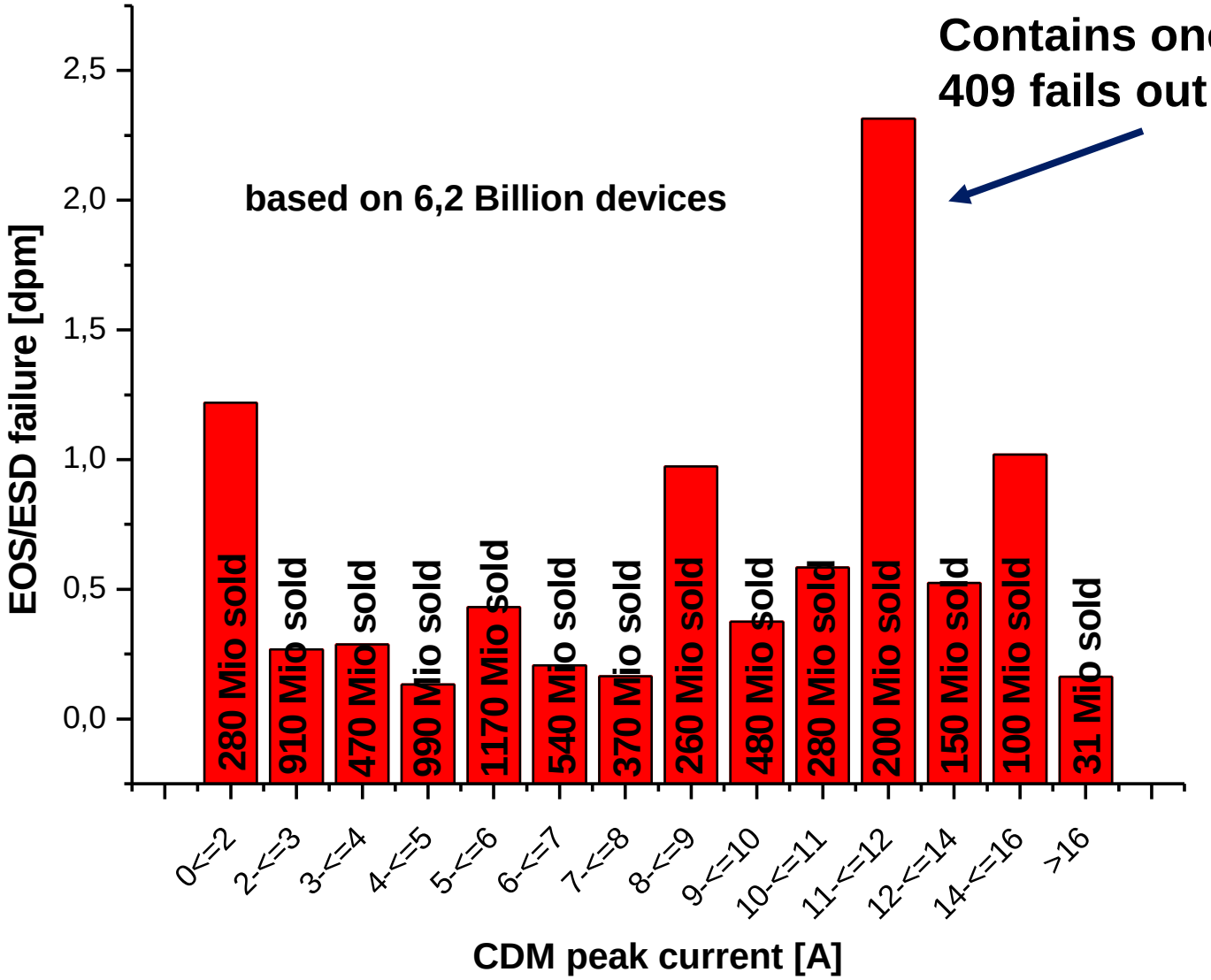
Visible or Accessible Internal I/Os

- Decreased risk when:
  - Signal net travels inside a PCB between the I/O and product internal interface
  - There are onboard protection components between the I/O and the interface

- Higher risks when:
  - I/O signal net is tested or contacted with pogo pins during frontend, backend, or PCB assembly phase
  - On-board connectors are connected to the I/O signal net during final assembly or testing
  - Cables are assembled to the I/O net during final assembly or testing

Evidence for CDM Targets Based on Field Returns Data

FAR Data versus CDM peak current

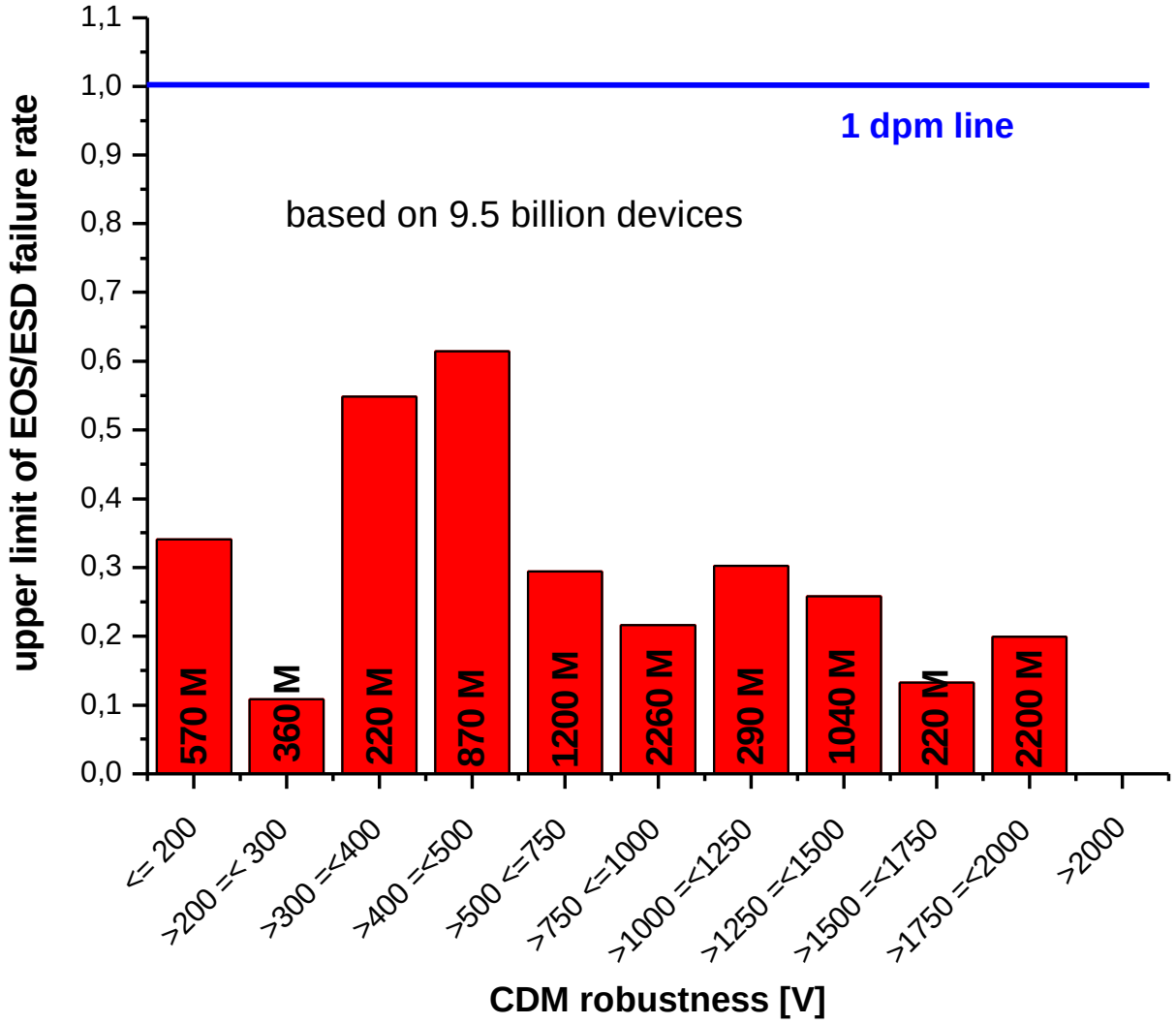


Limitations:

Some peak currents measured with 1GHz scope others with 4GHz scope (up to a factor of two difference in peak value)

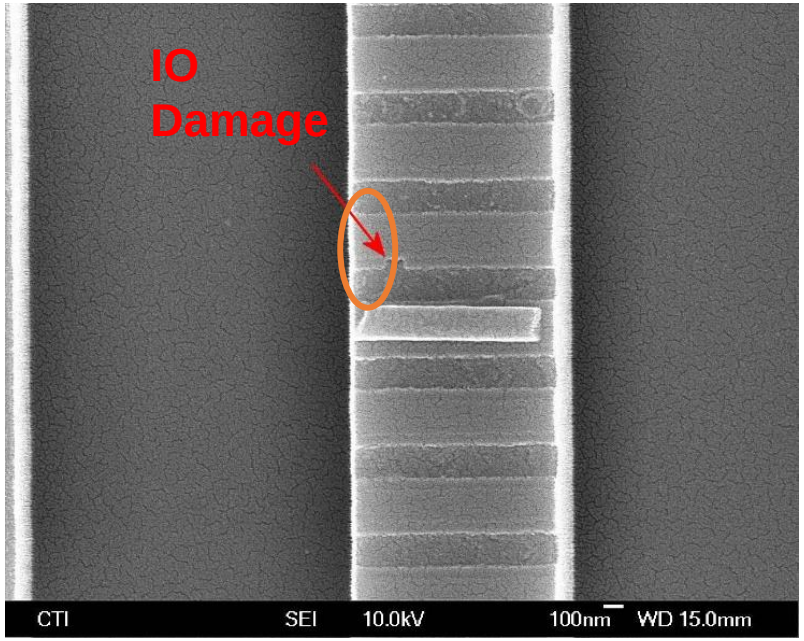
BUT: EOS/ESD failures occur at all CDM peak currents levels (even at very high values)

FAR Data versus CDM voltage w/o Outliers



- Important Observations:
  - Excludes 15 designs classified as FAR outliers (defined by > 100 field returns per type)
  - Remaining designs (934 out of 949) show a FAR rate < 1 dpm
  - No increase in the average return rate of parts with lower CDM level

Analysis of FAR of a CDM Weak Device



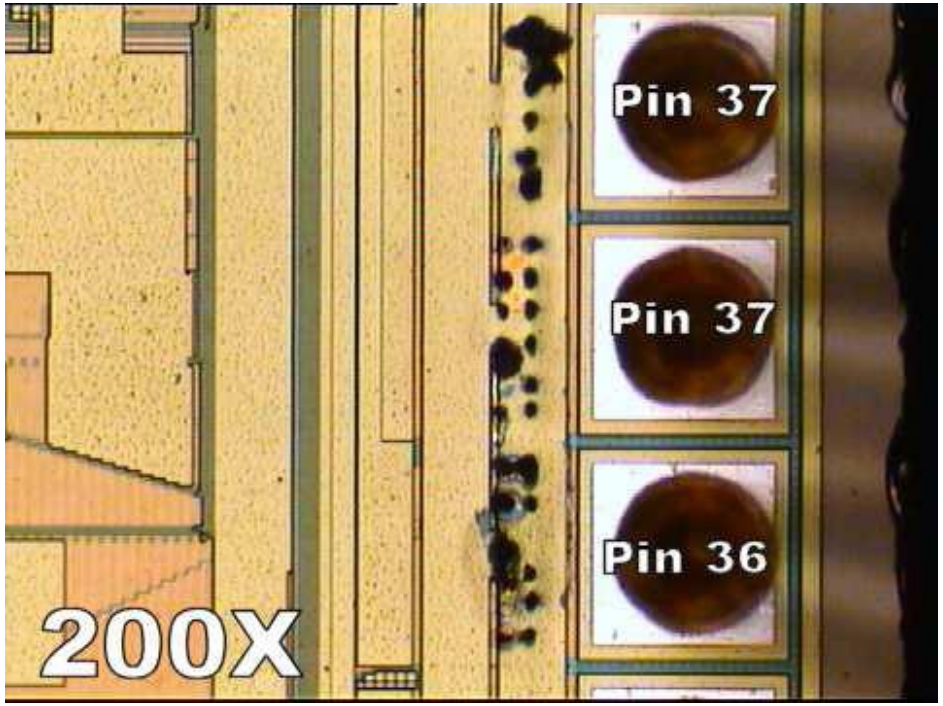
Design Issue & Failure Effect

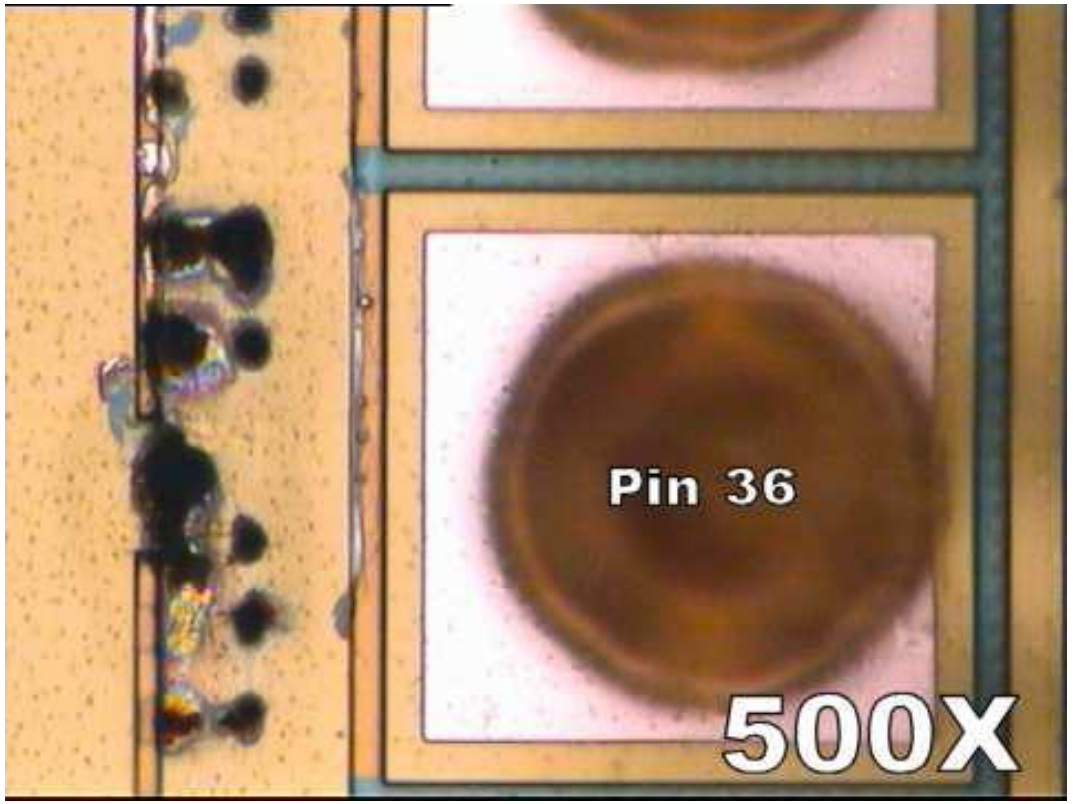
- high-speed IO performance required low capacitance ESD solution in 90nm
- Low capacitance solution = Low CDM
- Device pins were therefore clearly susceptible to field failures
- At the failure threshold current level for CDM discharge, IO damage is expected
  - FA indicated this expected damage

Low CDM Effect on FAR

- 140-Pin BGA shows 30 failures out of 67M units shipped
- CDM performance = <125V
- FA shows clear damage on IO gate due to marginal design
- Identical damage was detected on units stressed at 125V
- Implementing advanced CDM control resulted in 0 FAR for 105M shipped
  - Control measures can be effective even for low CDM

Analysis of FAR Outlier (CDM Robust Device)



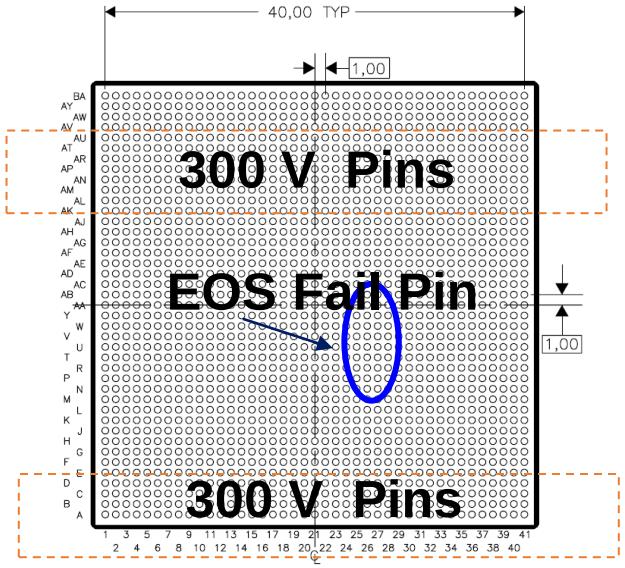


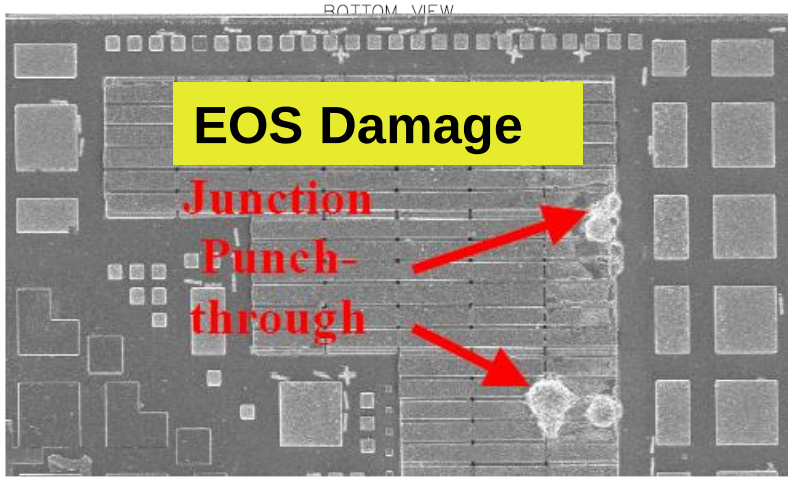
- Outlier in TQFP 100 shows 409 fails out of 36 M sold devices
- CDM robustness voltage = 1000V
- Failure showed molten metallization
- Failure is due to EOS but not CDM

Analysis of EOS related FARs

- Example of 130 nm product with medium CDM
- 1681-LGA Product has 320 high-speed pins
- 300 V CDM performance on all 320 HS Pins
- All other pins >500 V
- Some customer returns but with only EOS damage
- No EOS damage on any of the 300 V pins
- EOS on only Power Supply Pin with >500 V CDM

EOS on returns not correlated to CDM level





Conclusions from FAR Data Analysis (II)

- Case studies show that a number of field failures in the FAR data are due to EOS or Charged Board Events (CBE).
- There was no observed correlation of CDM weak pins and EOS fails.
- Due to the high energies involved, it is not possible to address EOS and CBE hazards by on-chip CDM protection design.
- CBE is a factory protection issue and must be addressed by assembly protection measures.

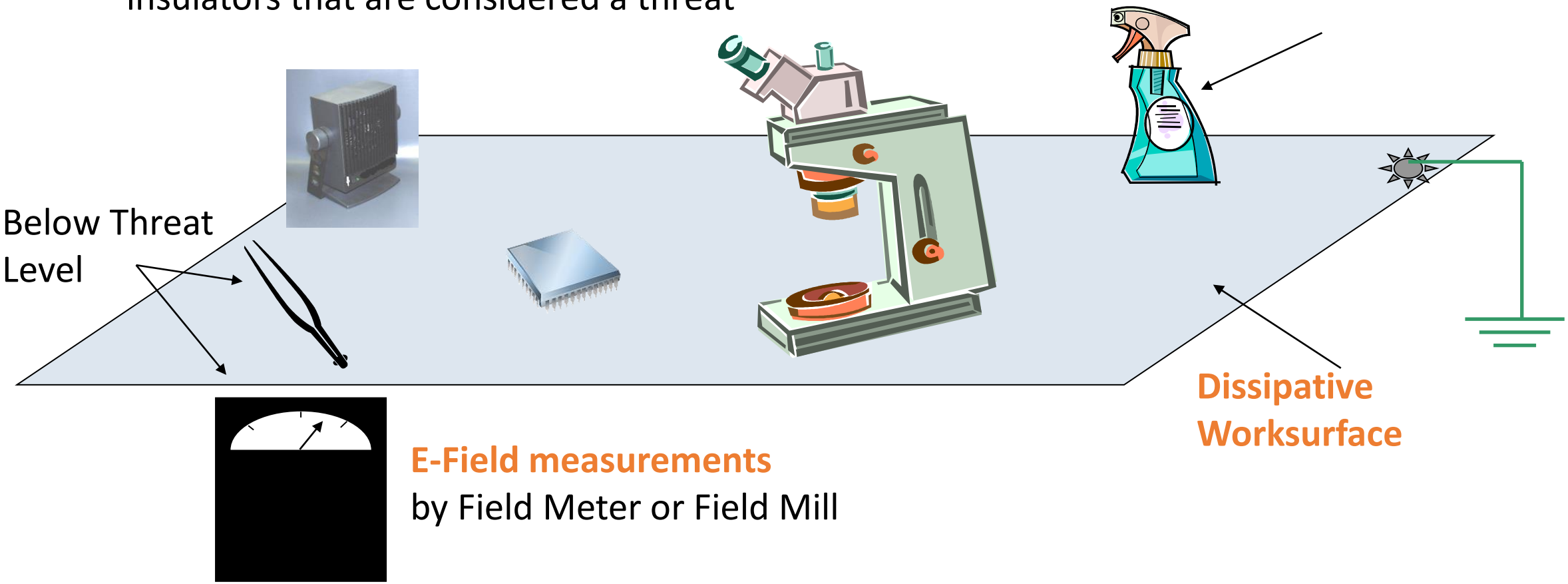
CDM qualification level should not be based on requirements against EOS and/or CBE.

Factory Control Strategies

Basic ESD Control Program addressing CDM

Ionizer if there are process relevant insulators that are considered a threat

Remove all non-process relevant **insulators**



E-Field measurements
by Field Meter or Field Mill

Threat level per ANSI/ESD S20.20 and IEC 61340-5-1

History of ESD Control for Safe Manufacturing

- For CDM, as with HBM, ESD control in the production areas is an essential part of a safe manufacturing process
- Effective ESD control measures covering CDM events include the grounding of metallic machine parts, control of metal-to-metal contact with the device leads AND control of insulators
- Control of insulators requires assessment of the various handling steps
- In principle, a detailed monitoring of each process step allows the handling of parts with very low CDM voltage even below 100 V
- IC level protection design has to comply to a safe minimum protection level set by ESD control in the ESD Protected Area (EPA), which limits the assessment effort when new handling processes are introduced

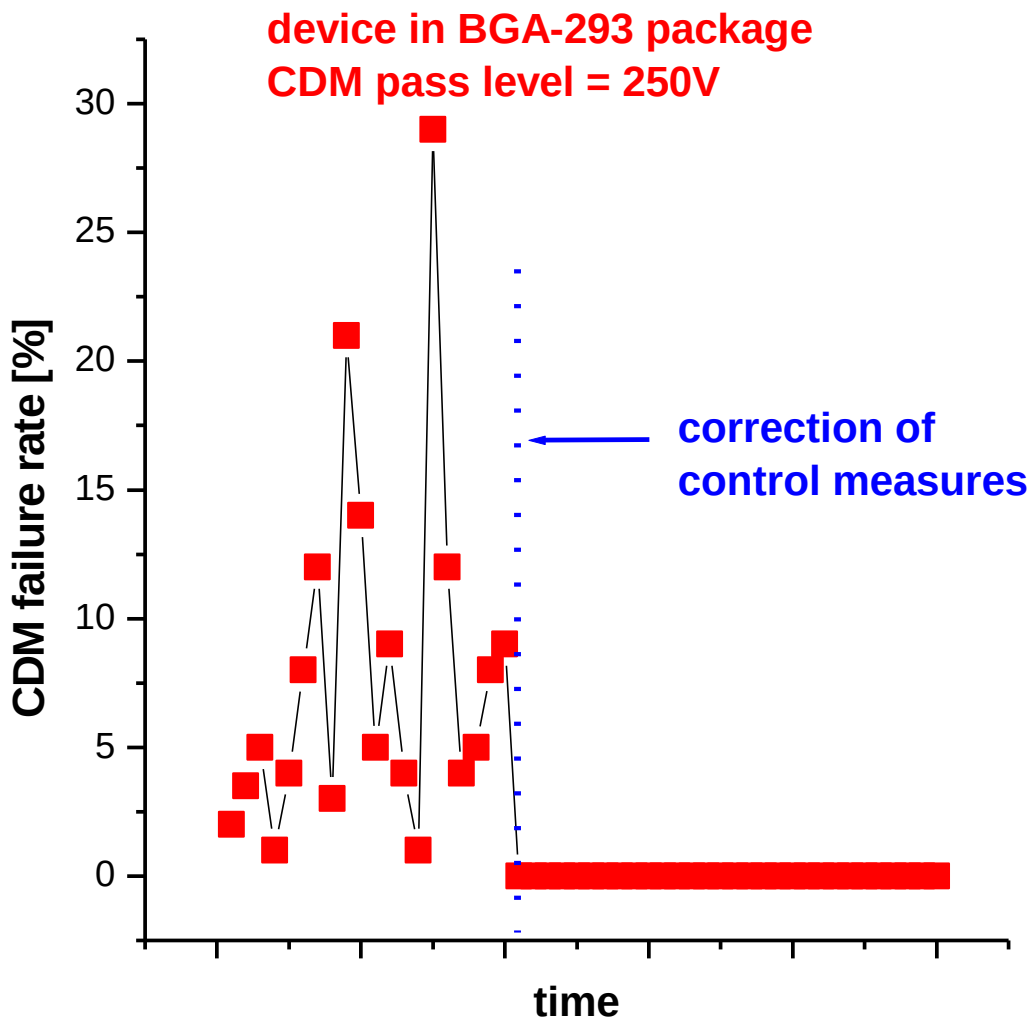
Summary – HBM vs CDM

- For HBM it is well known that with basic ESD control measures safe handling IC components can be guaranteed in an EPA
- But for CDM additional control measures may be necessary for specific handling processes in the EPA
- Therefore, for CDM a process-specific assessment to control charging of insulators in the manufacturing environment is required

Summary – CDM control

- Once this assessment has been done, the safe manufacturing of parts with very low CDM robustness is possible.
- The effort for the assessment and the tightness of control are related to the CDM level of the handled parts.
- Typically basic ESD control measures are sufficient to handle a device with a minimum CDM level of 250 V.

Confirmed CDM Failure @ Semiconductor Testing



- CDM fails may typically occur at the IC supplier site during a ramp-up phase
- These CDM fails can be removed with minor ESD control measure changes without any required IC design changes
- In this example:
  Ramp-up issue could be solved by an investment of
  < $ 1000

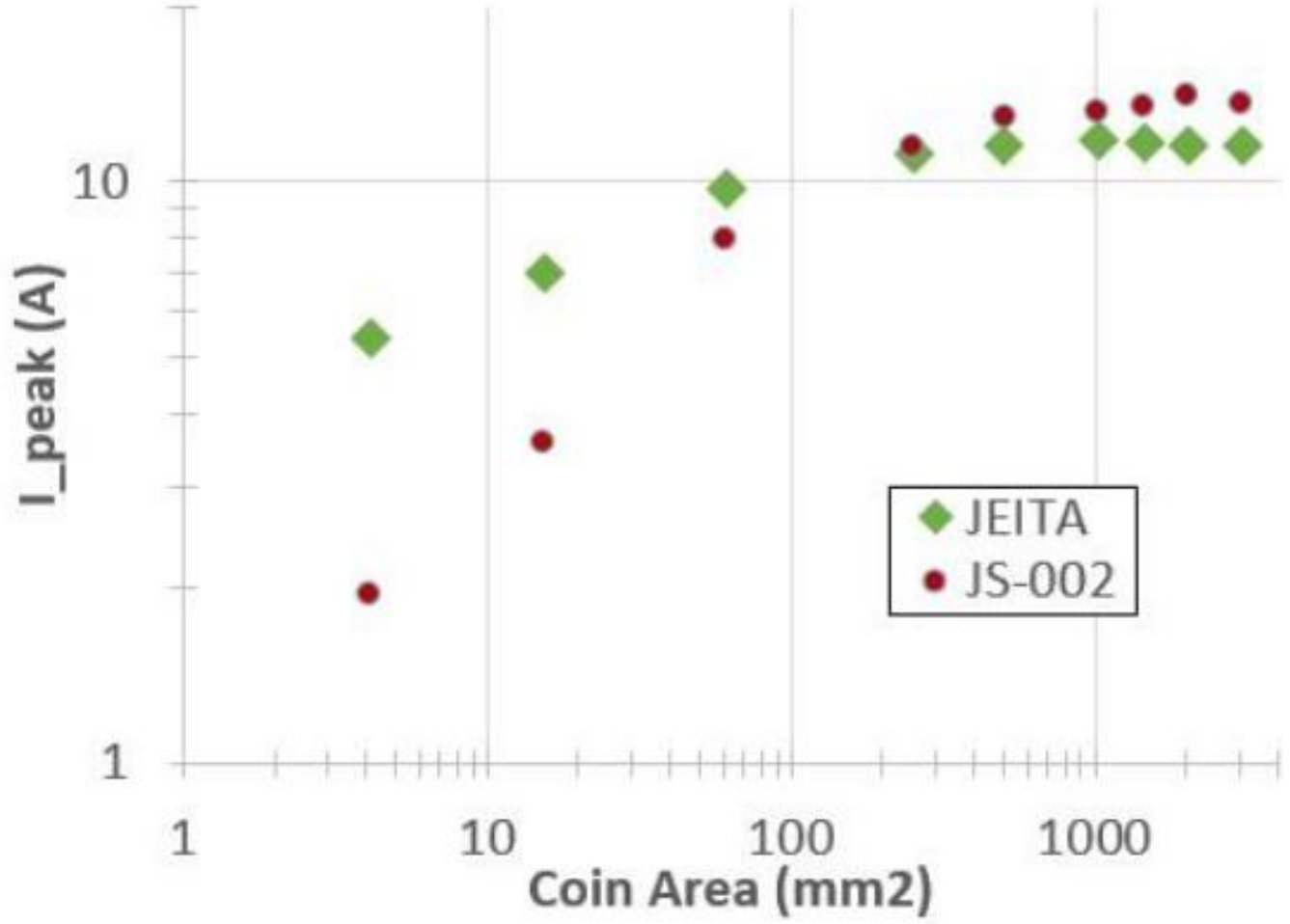
Example for CBE Failure of a CDM Robust Device

Failures with an automotive IC both in ECU production line, at '0 km' and in field.

- HBM ESD protection at ECU production was sufficient
- Several finished boards were electrically connected in a metal carrier
- Carrier had to be lifted for a special test to be isolated from ground.
- Carrier and boards got charged up to 250V.
- Discharge of all boards plus carrier through gate connection during test resulted in damage – although the device was CDM robust (>1000V)
- Due to limited test coverage damaged parts were shipped to the field – NO lifetime issue!
- Solution: grounding of carrier with a 10 MOhm resistance (Cost: 5 Cents)

Differences in CDM Test Standards

Peak Current's Dependence on CDM Standard



- Comparison of CDM standards including bandwidth of scope defined in standard
- Peak current of various CDM standards can vary by a factor >2 at same CDM voltage

Comparison of key CDM features of different standards

Organization	ESDA / JEDEC / IEC	AEC	JEITA
Standard	JS-002-2018	AEC - Q100-011 Rev-D	EIAJ ED-4701/302A 305D
Charging Method	Field-induced	Field-induced	Direct
Calibration Modules	Metal Coins	Metal Coins	Metal Coins
Calibration Module Thickness	1.27 ± 0.05 mm	1.27 ± 0.05 mm	1.3 ± 0.1 mm
Calibration Module Diameter	8.89 ± 0.127 mm (small) 25.4 ± 0.127 mm (large)	8.89 ± 0.127 mm (small) 25.4 ± 0.127 mm (large)	9.0 ± 0.1 mm (small) 25.0 ± 0.2 mm (large)
Calibration Module Capacitance	6.8 pF ± 5% mm (small) 55 pF ± 5% mm (large)	6.8 pF ± 5% mm (small) 55 pF ± 5% mm (large)	6.8pF, 55pF (Reference) (Not need physical dimensions due to adjust to the calibration current waveform)
Insulator Thickness (mm)	0.381 ± 0.038	0.381 ± 0.038	0.40 ± 0.04
Insulator Dielectric Constant	4.7 ± 5%	4.7 ± 5%	4.0 ± 5% (@ 1GHz)
Ground plane size	63.5 x 63.5 ± 6.35 mm	63.5 x 63.5 ± 6.35 mm	No specified shape and size (No shape and physical dimensions due to adjustment of the calibration current waveform)
Discharge	Air	Air	Relay
Current measured during CDM stress	Yes	Yes	Not required
Number of Discharges + & -	1	3	1
Number of Parts	3	3	3
Calibration Voltage Levels	125, 250, 500, 750, 1000	125, 250, 500, 750, 1000	125, 250, 500, 750, 1000

- Annex C demonstrating alignment to ANSI/ESDA/JEDEC JS-002 across nearly all of the industry