

White Paper 4: Understanding Electrical Overstress - EOS

Part II: A Novel Perspective on Transient AMR

Industry Council on ESD Target Levels



October 2026

Revision 1.0

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Abstract

This white paper on transient absolute maximum ratings (tAMR) is an extension of White Paper 4 on EOS [InCWP4] and the tAMR report from 2020 [InC2020]. It establishes a basis for mutual understanding of the maximum levels of transient pulses shared between semiconductor suppliers and system integration customers.

This white paper is intended to clarify the terminology of tAMR and its role in communication between an IC manufacturer and system developer. Both standardized, application-specific test methods and generic pulse characterization methods (such as transmission-line pulses) can provide data to enable an efficient, meaningful flow of information between the supplier and customer. The baseline for the discussion is that the system's stress robustness requirements do not equate to an equivalent stress at the IC pin.

This white paper presents a complementary framework for the limits of transient stress in regimes of reliability degradation and immediate damage under transient stress.

The white paper does not intend to define a qualification standard but rather to introduce terminology such as transient absolute maximum rating (tAMR) and acceptable transient stress area (ATSA) to support advanced system design and evaluation methodology. This is based on transient stress testing of the semiconductor component with a predefined stress event (see Chapter 1) agreed upon between the IC supplier and the customer for the IC. This testing can use simple techniques, such as a transmission line pulse (TLP), or leverage industry standards (see Chapter 2 and Appendix B) to generate the event. An example of a simple square pulse TLP to determine the ATSA is discussed (see Chapter 3).

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The goal was to set ESD requirements for integrated circuit (IC) products for safe handling and mounting in ESD-protected areas, while addressing constraints imposed by silicon technology scaling and IC design. The Council now consists of representatives from active full-member companies and numerous associate members from various support companies.

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Acknowledgments:

The Industry Council would like to thank all the authors, reviewers, and specialists who shared a great deal of their expertise, time, and dedication to complete this document.

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Mission Statement

The Industry Council on ESD Target Levels was founded on its original mission to review the electrostatic discharge (ESD) robustness requirements of modern IC products to allow safe handling and mounting in an ESD-protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by downscaled process technologies on practical protection designs, the Council provides a consolidated recommendation for future ESD target levels. The Council Members and Associates promote these recommended targets for adoption as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies.

In response to the growing prevalence of system-level ESD and EOS issues, the Council has expanded its mission to address one of the most critical underlying problems: insufficient communication and coordination between system designers (OEMs) and their IC providers. A key goal is to demonstrate and widely communicate that future success in building ESD robust systems will depend on adopting a consolidated approach to system design based on a clear and quantitative understanding of IC robustness. To ensure a broad range of perspectives, the Industry Council has expanded its roster of members and associates to include OEMs as well as experts in system design and testing.

Preface

In any business collaboration, the success of both parties depends on the commitment of each contributor to maintain a “Golden Standard” of cooperation and aligned specifications. Nonetheless, in a competitive environment, test results and specifications might be interpreted differently by different market players or across market segments. In this case, an industry alignment by collecting, documenting, and evaluating technical data from the field and introducing standards is essential for a productive market environment.

Typical examples of parameters that are often misinterpreted are absolute maximum ratings (AMR) and, specifically, transient absolute maximum ratings (tAMR). Where the term “transient AMR” has to be understood in the sense of “absolute maximum rating for a specific transient stress pulse”. A tAMR might not apply equally or affect design requirements equally across all customers or even across all designs over time from the same system manufacturer. It must be understood that a tAMR is specific to a particular situation and can only be set by the IC manufacturer.

Root cause analysis must determine whether the specification ratings were exceeded or whether the device failed to meet specifications when the device failed in the field or during production.

Invariably, conflicts can arise between IC manufacturers and their customers. The IC manufacturer, claiming an error on the part of the system designer, may rest on the suspicion that none of its other customers or designs using the failing device are having problems. The system designer, claiming a faulty IC, may also rest on the seemingly obvious issue that previous production volumes and batches of devices in the same design did not have any problems.

Both of these anecdotal assessments are potentially accurate, but not necessary or sufficient for placing blame, even when “ownership of the problem” should be joint custody.

The common understanding is that performance and robustness are assured up to a specification. However, any critical limit for a transient stress is even more difficult to extract due to its dependence on the specific nature of the transient stress. Any specification must be compared with diverse pulse shapes, repetition rates, and other complex contributors to failure mechanisms in the field. In addition, the functional state of a complex IC, such as a microprocessor, can have a critical impact on its response to a transient stress and its failure threshold, e.g., the change in breakdown voltage of a drain junction under different gate biasing conditions. This results in a much higher assessment complexity than, e.g., a two-pin discrete component. This requires detailed knowledge of IC behavior, which is only available on the IC design side.

The paper introduces the essential terms for meaningful communication between component suppliers and system developers (see Chapter 1). It provides an overview of standard test methods for transient stress conditions (see Chapter 2 & Appendix B) and discusses a TLP-based method for defining an acceptable transient stress area (ATSA) for a specific transient stress, using the example of a simple two-pin device (see Chapter 3). The latter is not related to specific system-level stress conditions and can only provide general guidance on the IC's robustness. It is useful if there is no direct interaction between IC design and the system customer during the early design phase (as with ASICs) and if the complexity of the IC pins to be characterized is low enough to give meaningful results. Finally, it provides an understanding of potential physical failure mechanisms, a description of these mechanisms, and the relevance of simulation methods under transient stress conditions to support root cause analysis (see Appendix A).

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group sponsored by JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD, reliability, and failure analysis experts from numerous semiconductor supplier companies. The data represent information collected for the specific analysis presented here; no specific components or systems are identified.

The Industry Council, while providing these recommendations, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

Glossary of Terms and Definitions

AC	alternating current
AEC	Automotive Electronics Council
AMR	absolute maximum rating
ASIC	application-specific integrated circuit
CDM	charged device model
CMOS	complementary metal-oxide semiconductor
CWG	combination wave generator
DC	direct current
DUT	device under test
EIPD	electrically induced physical damage
EFT	electrical fast transient
EM	electromigration
EOS	electrical overstress (relating to exceeding the AMR)
ESD	electrostatic discharge
EUT	equipment under test
FIT	failure in time
GND	refers to one particular point of many potential reference points, such as analog, digital, signal, shield, chassis, isolated, and Earth Ground
GOX	gate oxide
HB-LED	high-brightness LED
HBM	human body model
HCP	horizontal coupling plane
IC	integrated circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IP	intellectual property
IO	input/output
ISO	International Organization of Standards
JEDEC	Joint Electron Device Engineering Council
JEITA	Japan Electronics and Information Technology Industries Association
LED	light-emitting diode
LU	latch-up
ML	machine learning
MOC	maximum operating condition (upper limit of the SOA)
MOS	metal-oxide semiconductor
OEM	original equipment manufacturer
P2F	power-to-fail
PCB	printed circuit board
PKG	package
RC	resistor-capacitor network
RLCK	resistor-inductor-capacitor-mutual inductance network
RX	receiver
SEED	system-efficient ESD design
SPICE	simulation program with integrated circuit emphasis
tAMR	transient absolute maximum rating
TCAD	technology computer-aided design

TDDDB	time-dependent dielectric breakdown
TLP	transmission line pulse
TVS	transient voltage suppressor
TX	transmit
USB	Universal Serial Bus
VBUS	bus voltage
VCP	vertical coupling plan

Breakdown Voltage: the minimum voltage that causes an insulating material to become conductive or a diode to enter a high-conduction reverse state

Characterization: Quantitatively evaluating properties of a device

Damage: Permanent alteration of a device's properties

Device: Component

Discharge: A sudden, momentary flow of electrical current between two objects at different electrical potentials

Electrical: Relating to circuitry

Electromagnetic: Relating to electric and magnetic fields

Electrostatic: Relating to static electric fields

Emulation: Imitation of a system with physical methods, see simulation

Failure: A physical defect or an operation not meeting specifications

Junction: A bipolar boundary of semiconductor materials

Network: A system of interconnected elements

Optimization: Resolving parameters toward one or more ideal goals

Power: Instant or average dissipation (Volts x Amps)

Pulse: Transient electrical burst

Reliability: The capability of a system or component to perform its intended function consistently and without failure under specified conditions for a given period

Simulation: Imitation of a system with computer virtualization, often used to mean emulation

Stress: A physical or electrical condition, such as a physical force, voltage, or current, that can lead to damage or reduced lifetime

System: An interconnected network of components

Transient: Momentary variation in an electrical parameter like current, voltage, etc.

ATSA: Acceptable transient stress area defines the range of parametric transient conditions, such as voltage, current, power, energy, duration, etc., to which the device can be subjected **beyond the SOA** without immediate or latent damage or unacceptable degradation of the device's expected reliability profile for a limited time, significantly smaller than the targeted lifetime.

Note: Various ATSA excursion profiles beyond the regular operating regime may be defined for discussion between the component supplier and the system developer for specific application scenarios. These excursions represent conditions that, while exceeding normal specifications, maintain an acceptable reliability profile for particular applications when limited to transient events as mutually agreed upon by both parties.

LRTS: Lifetime reduction for transient stress defines the acceptable reduction in a device's expected reliability profile (lifetime) that component suppliers and system developers can negotiate to accommodate potential transient stress events during the system's operational lifetime. This reduction establishes a quantifiable trade-off between allowing specific transient excursions beyond normal operating conditions and the corresponding impact on long-term reliability.

Mission profile: The description of voltage, current, power, energy, and temperature over the full time of operation of the component. While it covers well-controlled operational states, transient stress should be included if there is system- or application-related repetitive transient stress. The mission profile is essential for evaluating lifetime compliance.

SOA: Safe operating area defines the range of parametric conditions, such as voltage, current, power, energy, duration, etc., to which the device can be subjected over its full lifetime while maintaining specified functionality and performance. The upper limit of the SOA is given by the MOC for those parametric conditions.

tAMR: Transient absolute maximum ratings are defined as a set of electrical limits describing the maximum transient voltage, current, power, energy, etc., **for a given waveform** at an IC pin or pair of pins, which should not be exceeded to avoid damage (including latent damage) or an unacceptable degradation of the device's reliability profile. The tAMR information can only be provided by the component supplier based on the customer's detailed stress scenario and waveform information and is provided to protect the customer from unintentionally damaging the product. The system developer (customer) can use the tAMR as a **reference** to establish the boundary conditions for transient stress events appearing in their specific system.

Executive Summary

Absolute maximum ratings (AMR) are specified physical limits for the storage, handling, and application of electronic or electrical products. They are specified and published by the manufacturer of these products, and they shall not be exceeded by the customer of these products under the worst probable conditions, in order to ensure the serviceability of these products. For integrated circuits (ICs), electrical AMR of IC pins is typically specified in terms of voltage, current, power, or energy. Reasonable AMR values are below the lower limit of the corresponding failure threshold and above the defined maximum operating conditions (MOCs). Any stress above the MOC and below the AMR is not expected to persist for an extended period; system reliability and lifetime are not guaranteed in that range. However, without further specification, the ‘extended period’ is undefined, and the AMR falls back to constant values. In fact, the AMR values provided in IC datasheets are often specified as constant (time-independent), which can leave system designers in a quandary when their systems involve unavoidable transient stress.

This document addresses critical technical issues arising from a misunderstanding of how AMRs are used. Many issues in this area can be resolved among the parties by first agreeing on strict definitions of seemingly obvious and innocuous terms, such as “absolute” and “failure.”

Introducing the concept of an acceptable maximum rating for a specific transient, called transient AMR (tAMR), is needed to help address this misunderstanding and support the design of systems exposed to transient events. As discussed in Chapter 1, Section 1.3, once the customer has identified a known aggressor pulse pre-design or an unexpected pulse post-design, the component supplier may be able to specify a tAMR, offering a unique opportunity for component suppliers and system integrators to collaborate and drive mutual success. The specification of tAMR values supports design decisions for system robustness. As a first step, the definition of terminology and an alignment of roles and responsibilities in the industry are required (see Chapter 1). An important clarification is the differentiation between the safe operating area (SOA) inside the boundaries of operation for the full lifetime and the acceptable transient stress area (ATSA) introduced as a new term to describe the parameter area of voltage, current, power, etc., outside of the SOA that envelops the transient stress but does NOT lead to immediate damage or an unacceptable degradation of the lifetime.

Standardized robustness stress tests provided by the International Electrotechnical Commission (IEC) or the International Organization for Standardization (ISO) are only applicable to the system test configuration for which they were defined (see Chapter 2 and Appendix B). While standard stress tests may not yield quantitative values for parameters used in system design simulations, they help assess a system's robustness based on experience with other components in the field. It is emphasized here that the qualification of the system's safe operation must be performed at the system level.

When assessing the electrical robustness of a semiconductor component, it is critical to understand the underlying failure mechanism, which can include gate oxide (GOX) degradation, electromigration-induced metal degradation, thermal damage, etc. (see Appendix A).

To support system design, the IC pin(s) can be characterized by applying a transmission line pulse (TLP) stress of an agreed-upon pulse length to extract stress-to-fail characteristics for a fast transient event. While TLP pulses may not always replicate the real-world event exactly, they can

still be a valuable tool for characterization. Additionally, reliability degradation can be modeled using aging models that address the relevant degradation mechanism at lower stress levels and longer stress times. This is shown in Figure 1, with the red curve indicating a limit derived by the manufacturer from reliability degradation for gate oxides and the blue curve representing the limit derived by the manufacturer from the power-to-fail behavior for fast current transients. The grey area can be considered the regime of acceptable transient stress for an agreed-upon pulse length (accepting a certain degree of lifetime degradation). This is defined as an acceptable transient stress area (ATSA) for square pulses for system design considerations (see Chapter 3). It is clear that this pulse testing cannot guarantee a robust level of component performance in a specific system exposed to widely varying stress waveforms. The system designer must be clear on what transient event needs to be characterized and communicate this to the component supplier.

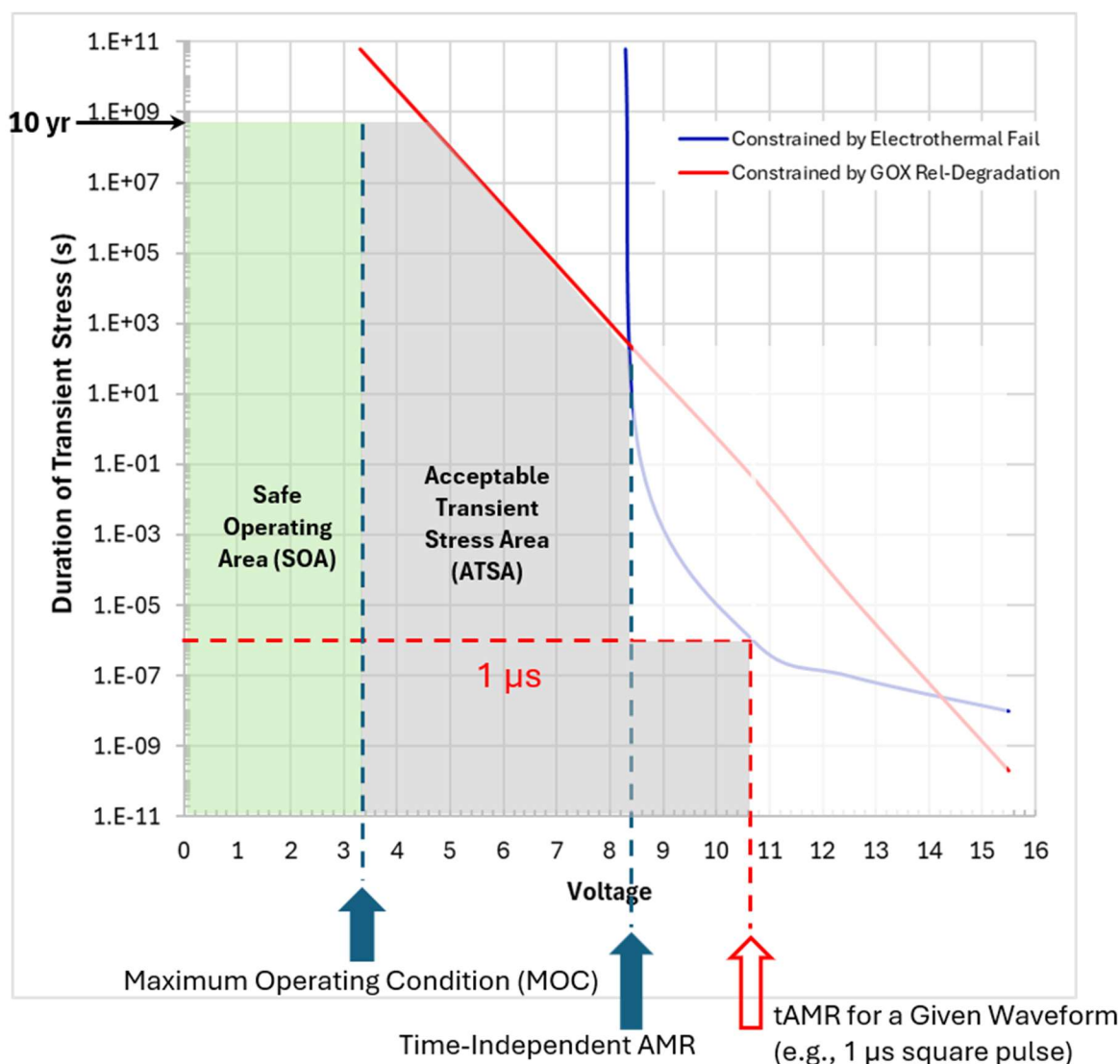


Figure 1: Reliability/AMR/tAMR Limits of a 3V3 Interface Containing an ESD Protection Element and a Gate Oxide (GOX) Structure

Note: The green area represents the region of safe operation with a guaranteed lifetime, while the grey area indicates the regime of acceptable transient stress, tolerating a certain degradation of lifetime. The region of acceptable transient stress for a 1 μ s short square pulse is shown. This is limited by the transient AMR parameter for this specific waveform.

Frequently Asked Questions

Q1: What is tAMR?

A1: tAMR (transient absolute maximum rating) is defined as an electrical parameter describing the maximum transient voltage, current, power, energy, etc., and duration for a given waveform at an IC pin or pin pair, which should not be exceeded to avoid damage (including latent damage) or an unacceptable degradation of the device's expected reliability profile.

Q2: How is tAMR different from SOA?

A2: SOA (safe operating area) defines the range of parametric conditions, such as voltage, current, power, energy, etc., and duration, to which the device can be subjected over the whole lifetime while complying with specified functionality and performance (see Chapter 1 for a graphical representation).

Q3: What is ATSA?

A3: ATSA (acceptable transient stress area) defines the range of transient parametric conditions (for example, voltage, current, power, energy) and duration to which the device can be subjected beyond SOA without immediate latent damage or unacceptable degradation of the device's expected reliability profile.

Q4: Then how is ATSA related to tAMR?

A4: ATSA defines the area within Region B (see Chapter 1) below the AMR/tAMR boundary, where an acceptable reliability degradation profile is maintained.

Q5: If I exceed AMR in my application, does it mean immediate damage to the product?

A5: It's possible. Exceeding AMR does not always result in immediate failure or damage. Beyond AMR, there is a risk of either latent (Region C) or immediate (Region D) damage.

Q6: What does the AMR value documented in the datasheet represent in field conditions?

A6: AMR values are often specified as time-independent and are pin or product-specific. However, there are market segments where a time-dependent AMR is specified.

Q7: What are the risk factors that impact components?

A7: The amount and duration of stress have an impact on the risk.

Q8: If AMR is important for what it is, then why should I worry about this “transient-AMR”?

A8: AMR is defined in a datasheet, but does not always specify the duration of this stress. Excessive stress beyond a time-independent AMR might be tolerated, but it is unclear for how long, thus requiring studies of tAMR.

Q9: Is tAMR considered a safe boundary for the operating limits of a component?

A9: No. tAMR intends to clarify the boundary between Regions B and C (latent damage) as a function of a specific time interval. See Chapter 1.

- Q10: Can tAMR be considered as an alternative to a time-independent AMR rating?
- A10: No. tAMR cannot be used as a substitute for a time-independent AMR; tAMR can be considered as a complement to the time-independent AMR, as tAMR is supplied by the component supplier for a specific transient event agreed on with the customer. tAMR is being introduced to provide a greater understanding of the short-term limitations in the behavior of components beyond normal operating voltages and currents.
- Q11: Why not create a defined specification for tAMR to avoid confusion regarding this requirement?
- A11: While a time-independent AMR spec can be defined at the discretion of the supplier, it is much more complex to specify a tAMR value since, without any defined transient event to work from, it would involve characterizing a large number of pulse shapes, how pulse repetitions encounter the device, or even the IC operating status. This complexity makes it nearly impossible to proactively supply a tAMR for components and only allows for a tAMR to be supplied once discussions of possible transient events have occurred between the component supplier and customer.
- Q12: If component suppliers define a time-independent AMR value, who decides on the tAMR specification?
- A12: As a subset of the time-independent AMR, a tAMR is also defined by the component supplier. A component supplier may be able to provide a tAMR characterization of a component only after communication between the system developer (customer), who provides details of the stress scenario, and the component supplier, who can then provide a tAMR based on this information.
- Q13: Are human body model (HBM) and charged device model (CDM) stress tests also tAMR considerations?
- A13: HBM and CDM withstand thresholds are given in the datasheets. HBM and CDM withstand thresholds are examples of specific transient events to which a device can be subjected, with threshold limits set for a manufacturing environment; the related electrical parameters, such as voltage or current at the IC interface pin, could therefore be considered a tAMR for that event.
- Q14: Are “time-independent AMR” and “tAMR” new datasheet parameters?
- A14: No. AMR is the only datasheet parameter. The term “time-independent AMR” is only used in this document to better distinguish conventional AMR from “transient AMR (tAMR)”. Transient AMR is a concept for discussion between the IC manufacturer and the system developer, using the IC under limits applicable to a defined number of brief transient stress pulses with a specified shape. It is not a datasheet parameter.

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Chapter 1: Concept of tAMR – Terminology, Roles, and Responsibilities

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1.1 Introduction

Absolute maximum ratings (AMRs) [InCWP4] are well established as critical for minimizing electrical overstress (EOS) incidents and related damage. In this document, we will use “time-independent AMR” for AMR to better distinguish it from “transient AMR (tAMR)”. The phrase time-independent AMR represents “conventional AMR applicable to relatively long stress duration”. The phrase transient AMR represents “AMR applicable to a defined number of brief transient stress pulses with specified shape”. Neither phrase defines a new datasheet parameter. A device’s AMR is often defined as time-independent, in which the AMR values specify the maximum limits to which a device can be subjected without immediate or latent damage. It also serves as a warning that operating above the AMR can result in electrically induced physical damage (EIPD).

Consider now a 5-volt nominal device with a maximum operating voltage (V_{max}) of 5.5 volts whose time-independent AMR specifies a maximum of 6 volts on an input/output (IO) pin. When in the field, the IO experiences a transient event up to 7 volts. While the time-independent AMR limits are exceeded, the device may operate normally during and after the transient event. Typically, the shorter the transient, the larger the failure threshold at which EIPD damage can occur. Such transient violations of the time-independent AMR can vary in duration and magnitude. If the device survives, it likely did so because the transient event did not exceed its failure threshold.

The motivation for this document is the industry's existing ambiguity regarding the understanding of AMR for transient stress. The existing definitions, such as IEC 60134 [IEC60134], have largely been ignored by suppliers and customers, and are needed to avoid misinterpretation or reduce the number of EOS findings in the field. The overall scope of this document is to provide a clearer explanation of tAMR phenomena, build a foundation for mutual understanding between component suppliers and system designers regarding the transient pulse parameters that affect system reliability, and offer options for achieving robust system designs.

So, what is a tAMR? tAMR is the manufacturer-specified, waveform-specific maximum stress level that a device can withstand for limited transient conditions, without immediate damage, latent damage, or a reduction of the acceptable lifetime. In most system applications, the typical transient stress pulse is shorter than one second. However, repetitive transient stress conditions can accumulate, leading to significant lifetime reduction even at lower stress amplitudes. In any case, the reduction may not exceed the lifetime reduction for transient stress (LRTS).

Recent surveys indicate that many in the industry do not fully understand AMR specifications as a general concept. The addition of unknown transient pulse events that exceed time-independent AMR values only compounds this lack of understanding. A quick review of the operating regions follows to refresh the reader on time-independent AMR and its application. In Figure 2, four regions of operation are defined.

Acceptable transient stress areas (ATSA) and tAMR can provide a framework for a clearer, waveform-specific characterization and communication of transient stress limits beyond traditional time-independent AMR, enabling component suppliers and system designers to collaborate more effectively on realistic boundaries for application-specific aggressor pulses in real-world systems. By understanding ATSA and LRTS, system designers can reduce ambiguity, minimize misinterpretations that lead to unnecessary over-design or field failures, and support optimized system designs that balance cost and performance, without compromising reliability and safety.

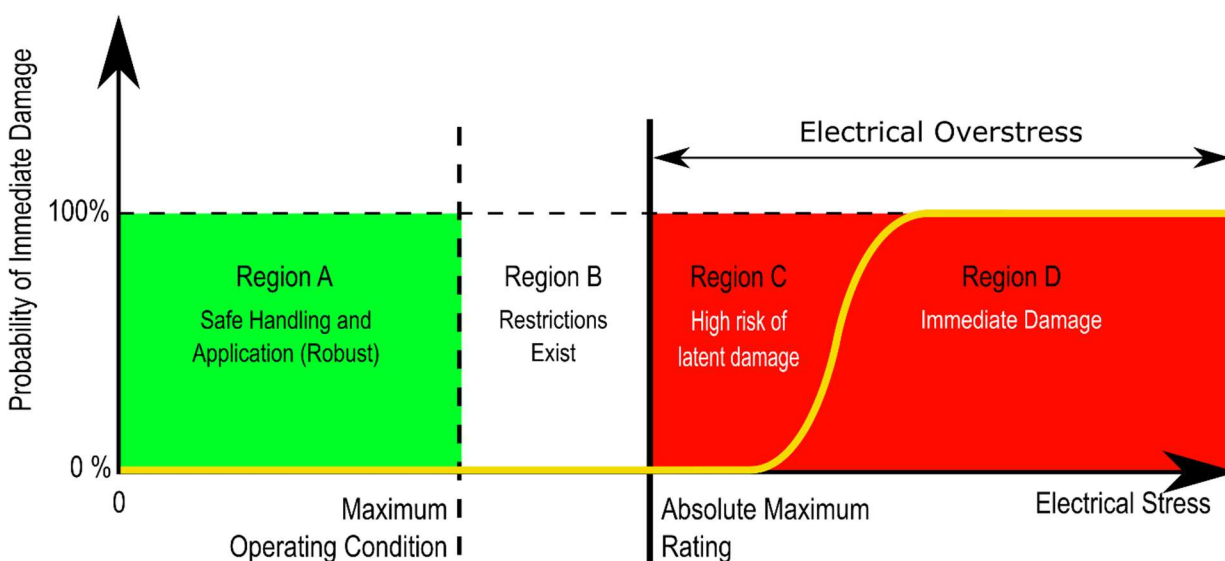


Figure 2: A Depiction of How Absolute Maximum Ratings Should be Interpreted
Note: The yellow line is the percentage of components suffering immediate, irreversible damage.

The operation of a device in these four regions is described as follows:

- Region A: The safe operating area. Handling or operating a device in this region does not come with additional reliability restrictions or limitations.
- Region B: This region is negotiable, and the user should approach operating here with an understanding of the effects. For example, in this region, the device may not be guaranteed to function as specified and may also suffer reliability issues such as reduced product lifetime. This region can be quantified more precisely using ATSA. ATSA and tAMR can provide a framework for a clearer, waveform-specific characterization and communication of transient stress limits beyond traditional time-independent AMR, enabling component suppliers and system designers to collaborate more effectively on realistic boundaries for application-specific aggressor pulses in real-world systems. By understanding ATSA and LRTS, system designers can reduce ambiguity, minimize misinterpretations that lead to unnecessary over-design or field failures, and support optimized system designs that balance cost and performance, without compromising reliability and safety.

The right-side limit of Region B is the AMR. To the right of this region are two areas of EOS:

- Region C: Operation in this region will result in a high risk of latent damage.
- Region D: Operation in this region results in immediate EIPD.

These two areas are divided by a yellow line. This line shows the percentage of parts experiencing immediate EIPD and illustrates the transition from latent to immediate damage. The line's shape is the result of normal process variation.

As noted above, transient stress pulses limit the power dissipated or energy transferred to the device: the shorter the transient, the larger the failure threshold. Consider the depiction of transient stress pulses in Figure 3.

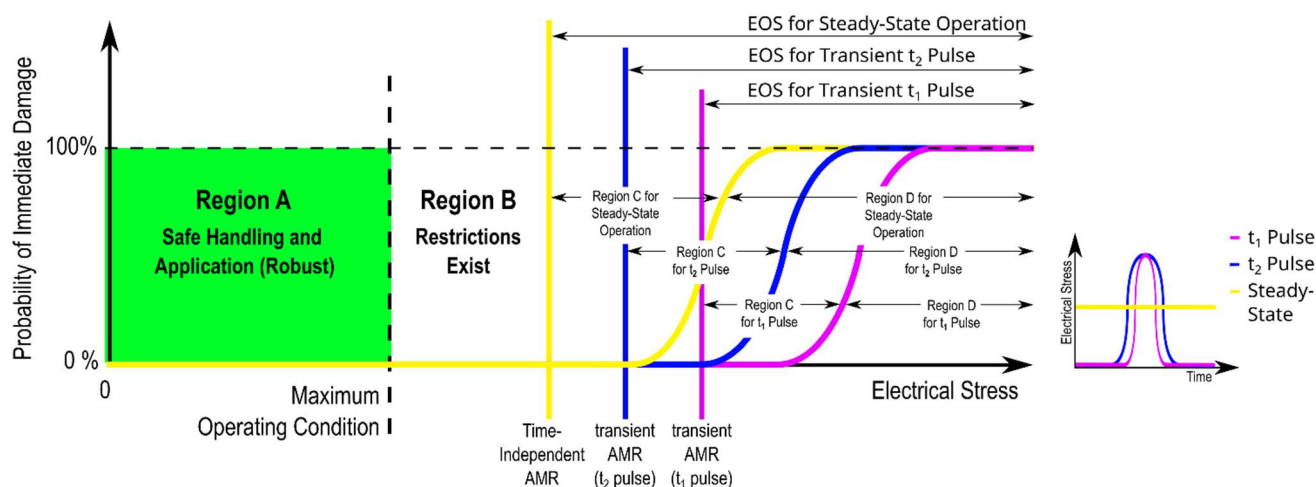


Figure 3: A Depiction of the Probability of Immediate Damage Versus the Pulse Duration (with $t_1 < t_2$) [InC2020]

Here, the time-independent AMR and its Regions A and B are unchanged. However, if the failure threshold depends on pulse duration, then shorter pulses will increase the failure threshold. An illustration of this is shown in Figure 3, where the blue curve shows a short transient pulse, and the magenta curve shows an even shorter one. Intuitively speaking, this might seem reasonable, but is it a realistic or accurate assumption?

In reality, the curve between Regions C and D with shorter transient times does not necessarily shift in a parallel fashion, such as those shown by the blue and magenta solid curves. The shape of such a curve and any shift due to pulse duration must be determined through a detailed analysis of relevant field studies, which must include data on various transient conditions. Among the major failure mechanisms of semiconductors, there is a general trend that the failure threshold increases as the stress duration decreases (in fact, no major failure mechanism with the opposite characteristic is commonly observed). There are complex parameters involved, such as the minimum stress required to cause thermal damage, breakdown voltage of dielectrics, power-to-failure versus pulse width (Wunsch-Bell relation) for specific case studies, and an understanding of statistical reliability models, their limits, and regions of application. This results in a complex picture of tAMR, and it must be acknowledged that a universal description of tAMR for arbitrary stress situations is not possible.

In simpler devices, characterization of failure thresholds with simple square pulses (e.g., TLP) can give meaningful results. The more complex the integrated circuit's internal topology connected to the external IC pin, the less likely it is that an isolated characterization of that pin using simple square pulses (e.g., TLP) will yield comprehensive, meaningful results.

1.2 Expectations Regarding Defining and Implementing tAMR

This section discusses questions about what is and is not addressed by regimes defined for transient stress. Defining a time-independent AMR and a tAMR provides a recommended margin for operating a semiconductor component beyond normal system operational conditions. It is based on an assessment by the component supplier that considers manufacturing process variations, statistical spread, and aging conditions. Exceeding it does not necessarily imply immediate and obvious failure of or damage to any particular part, as latent damage can occur. Stress-to-fail experiments for AMRs require a statistically significant sample size to account for physical damage mechanisms, such as SCR triggering or dielectric breakdown, which depend on transient waveforms. The system designer cannot calculate any AMR based on a few stress-to-fail experiments, especially when determining tAMRs where various physical damage mechanisms, such as triggering of silicon-controlled rectifiers or bipolar devices, as well as dielectric breakdown, depend on the transient waveform and must be considered. This derating methodology (see Section 3.4) can guide the definition of an ATSA for a specific application with a modest sample size, but specific sample sizes and test details should be determined in consultation with reliability engineering experts within the company.

This document introduces the terms ATSA and tAMR. These are determined by the component manufacturer to enable the use of system simulation during the system design process. It explains why, under short transient stress conditions, the tAMR value is higher than the time-independent AMR value under steady-state conditions. Also, unlike certain standardized stress tests (see Chapter 2 and Appendix B), where the waveform (pulse) is defined, ATSA and tAMR cannot be determined until the customer has identified a known aggressor pulse pre-design or an unexpected pulse post-design (see Section 1.3). The standardized tests discussed in Chapter 2 and Appendix B are requirements referenced in the contract between the supplier and the customer. The system designer can expect the design to be robust to limited excursions within the tAMR limits, but it should be noted that the margin to a failure threshold has been reduced, and in some cases, significantly. However, this limited excursion must be validated by stress testing of the complete system hardware under the stress conditions typical for the specific application. On the other hand, neglecting these tAMR limits during system design can lead to a high risk of field problems. Beyond the system design phase, the provision of tAMR could enable faster debugging and root-cause analysis in the event of field failures due to transient stress.

With this concept in mind, a characterization of a component's transient stress regime can be developed through stress testing. This can be testing of a stand-alone device or a device mounted in a standardized system or printed circuit board (PCB) configuration. It is important to differentiate between the so-called **safe operating area (SOA)**, which is referred to as the parameter regime where the device can be **operated fully functional over the full specified lifetime** and a newly coined term of an **acceptable transient stress area (ATSA)**, which describes the parameter region where the device is stressed outside SOA and **doesn't suffer latent or immediate physical damage or degrades its lifetime beyond an acceptable margin**. It should

be emphasized that the use of SOA is often ambiguous, for example, in bipolar or high-voltage devices, where it refers to the region before breakdown and thermal runaway. The use in this document is in the narrower sense of compliance with a full operating lifetime. ATSA describes the robustness margin for a targeted transient stress or, if repetitive stress is relevant, integrated stress durations. A representation is shown in Figure 4.

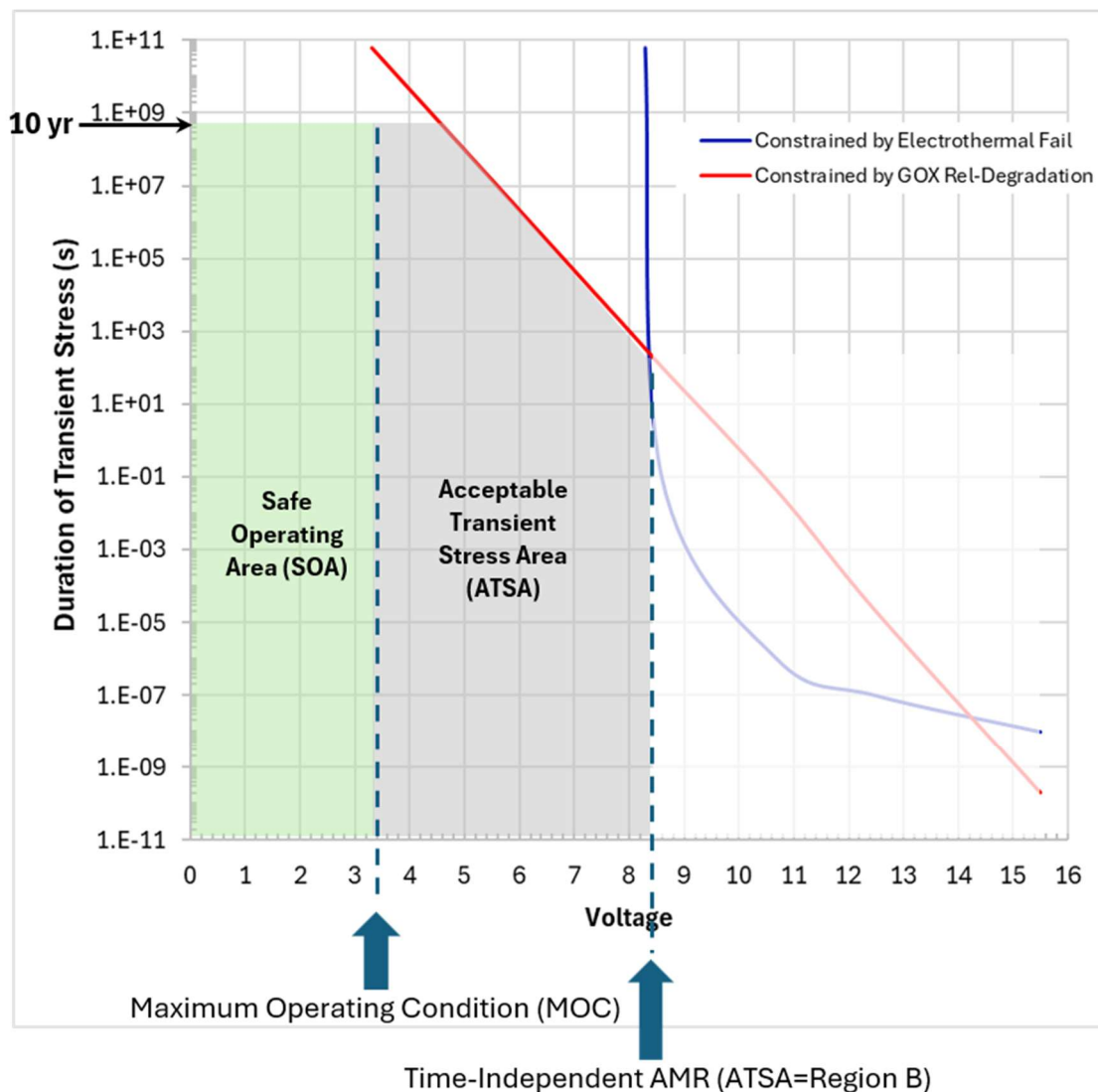


Figure 4: Reliability/AMR Limits of a 3V3 Interface Containing an ESD Protection Element and a Gate Oxide (GOX) Structure Defined by the Time-Independent AMR

Note: The green area represents the region of safe operation with a guaranteed lifetime, while the grey area indicates the regime of acceptable transient stress, tolerating a certain degradation of lifetime.

The “duration of transient stress” indicates the integrated duration of the transient applied to the electronic device in the case of limitation by reliability degradation. To extract ATSA, the component supplier and the system integrator must reach an agreement on the acceptable degradation of the lifetime. This is referred to as a lifetime reduction for transient stress (LRTS). Knowing LRTS and the type of transient stress, the ATSA of the electronic device can be

characterized. The ATSA characterization of the specific waveform of a square pulse is discussed in Chapter 3. The tAMR is now defined as the threshold for a very specific waveform of a defined duration. As such, it is one data point of the envelope curve of an ATSA characterization.

Characterization of ATSA and tAMR is applicable to any pulse-generation method appropriate to the application. Examples may include, but are not limited to, transmission line pulsing (TLP), combination wave, lumped element, or other waveforms. A surge pulse with a slow rise time (e.g., damped sinusoid) may not have the same reliability effect on an input capacitor dielectric as a fast rise time square pulse, even at the same energy or power level. If a pulse type (or a set of pulse types) is found that more closely matches the real-world stress pulse(s), it is generally a more suitable choice than a generic test method such as TLP. In no case is it reasonable or possible to generalize characterization results of a particular characterization pulse to all possible aggressor pulse shapes. Pulse-emulation type, severity, reasonable application modes and limits of characterization, etc., are all elements to be negotiated between component suppliers and system integrators during this analysis.

A critical aspect of extracting tAMR values and the ATSA region is accounting for process variation and statistical distributions. Due to limitations in sample testing, the engineer on the component side needs to decide on the envelope that safely encompasses the behavior in high-volume production, resulting in a test of limited size. This is the component supplier's full responsibility and must be understood by the system design team.

1.3 Roles and Responsibilities: Fostering Collaboration for Optimal Results

In the electronics industry, a harmonious partnership between component suppliers and system integrators is best for achieving optimal performance, robustness, and cost-effectiveness. While the dividing line between these entities may vary across industries, it is essential to acknowledge the importance of collaboration and clear communication.

The implementation of ATSA and tAMR offers a unique opportunity for component suppliers and system integrators to collaborate and drive mutual success. By embracing tAMR principles, partners can establish clear definitions, optimize system designs, and ensure products meet the required standards for performance, robustness, and reliability at the most reasonable overall end-product cost.

While the ideal roles are outlined here, with typical capabilities understood (component suppliers understand semiconductor reliability and system designers understand their particular power delivery network and IO application environment), we recognize that responsibilities may be most efficiently allocated to the appropriately capable assets. A component supplier's application engineering group, for example, may have more system-level characterization expertise than its customer, and a system integrator may have more real-world reliability experience than the component supplier. Nevertheless, acknowledging the importance of partnership and open communication, all parties can benefit from more satisfying end-user experiences.

Application of tAMR concepts typically occurs in one of two main scenarios:

- (1) Pre-design/ideal planning stage, where, early in the process, the customer provides definitions of aggressor pulses that the IC should be able to survive, allowing the component supplier to proactively design the device to handle them. This is the desired and most reasonable approach.
- (2) Post-analysis or field-failure “catch-up” mode, where the customer presents a new, unexpected pulse and requests reliability certification, often superimposed on a running product cycle where new pulse requirements identified in the field become desirable for next-generation designs.

In much of the industry, these phases run concurrently within cyclical, cross-organizational processes. When a product receives field feedback during its post-analysis phase, that design information can be applied to a next-generation design in the pre-design phase. An “internal customer”, such as internal applications or product marketing groups, may provide proactive new applications or new market conditions that merge the two phases into a competitive advantage before the “external customer” is even aware of the issue.

For example, in the automotive sector, component suppliers and system designers should work closely together, with the latter relying on the former for support in problem resolution. This collaboration enables the development of high-quality products that meet stringent safety and reliability standards. Cooperation and shared responsibility for problem-resolution actions will typically yield better solutions than simply demanding that either the component supplier or the system designers make a change. At the very least, understanding and sharing a common problem definition is a good step toward stronger collaboration.

In contrast, the consumer electronics industry may present a different scenario, in which system designers may have limited visibility into the component supplier's design, characterization, or processes. However, this does not diminish the potential benefits of collaboration. By working independently and sharing knowledge on the reference problem definition, both parties can eventually create innovative solutions that can exceed customer expectations.

When deciding whether to specify ATSA/tAMR (especially for complex chips), the key questions are whether a reasonable effort will yield meaningful results (i.e., results that are valid and useful for the specific application) and what results are reasonable from an economic and practical standpoint. “Simple” (e.g., 2-pin TVS) vs. “complex” (e.g., integrated servo-driver, motor-controller, CPU, etc.) topologies influence meaningfulness first; high-stakes scenarios (e.g., recall avoidance or quality feature for a next-generation product) may justify the effort despite cost and difficulty, while others may not. Origins of absolute maximum ratings driven by process constraints (and not merely copied from competitor specs) may differ from the motivations for specifying tAMR or ATSA, given cost, safety, and reliability considerations (e.g., aging, use case).

However, the decision to pursue or not pursue specifying tAMR/ATSA on a particular device, as outlined in this document, may reasonably consider business conditions, resource availability, and other economic realities. System designers should consider this specification as they would any other feature or capability with cost/performance tradeoffs, and not part of a uniform quality or acceptance line item expected for every product.

Chapter 2: An Overview and Motivation of Standardized Test Methods in Various Industries

Andrea Boroni, STMicroelectronics
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2.1 Introduction

Reliability tests are conducted on all aspects of a system, from individual devices and components to the complete system, to ensure optimal performance throughout the entire lifespan of the final system. Some are designed to evaluate the effects of aging, while others are targeted at understanding system responses to external aggressors, which range from mechanical stress to electromagnetic interference.

Reliability trials can have two different scopes: a single device and a system or part of it. For this reason, norms can be divided into device-level and system-level standards.

At the device level, testing is a combination of unpowered and powered stress tests. The assessment of failure is based on automated test equipment testing and performance drift evaluation before and after the stress. On the other hand, at the system level, most tests are powered.

There are generally four levels of failure for a system:

- The system cannot continue to perform properly.
- The system needs to be manually cycled to recover its functionality.
- The system self-reboots.
- The system loses function, or a performance degradation occurs that is eliminated after the disturbance ceases.

The scope of this chapter is to focus on transient electrical stresses (either voltage, current, or power) that can lead to immediate or permanent malfunction of a system or part of it.

2.2 Transient Stress Tests at the Device Level

Device-level stress limits have been included in device datasheets (often in the AMR section) for a long time, but there are still differences in how the limits are reported. There are also different test methods and expected passing levels depending on the targeted industry segment. For the same failure model, all standards refer to the same aggressor waveforms. A device is considered a failure if it fails to meet one or more parametric or functional testing criteria defined by the product manufacturer.

The purpose of ESD test standards is to ensure the devices can be handled without damage during manufacturing and to identify devices that may require special care. The connection between device-level robustness and system robustness is complex. Device-level robustness can improve system robustness or have no impact on system robustness at all. There have even been cases in which increased device-level robustness has resulted in poorer system-level robustness.

The most commonly used standards to characterize the robustness of devices against the most common ESD transients during manufacturing are:

- ANSI/ESDA/JEDEC JS001 [JS001] – “Human Body Model (HBM) Device Level”.
- ANSI/ESDA/JEDEC JS002 [JS002] – “Charged Device Model (CDM) Device Level”.

In addition, JEDEC JESD78 [JESD78] stress testing is required for device qualification to assess robustness to operational disturbances. Different pulses are applied to a single device (three devices in total are stressed), but in this case, the device is powered, and a failure is defined as a measurable increase in current drawn from any pin of the device.

2.3 Transient Stress Tests at the System Level

System-level stress standards are intended to mimic aggressor pulses that can affect the system throughout its lifespan, so they depend on the environment in which the electronic device is intended to operate and, consequently, on the industry segment. Because of the variety of possible scenarios, there are several different standards; the pulses described are meant to simulate situations ranging from human handling for consumer applications to inductive noise for industrial applications up to lightning for the avionic market.

The most common test among the industries is IEC 61000. The IEC 61000 specifications define a set of electromagnetic compatibility (EMC) immunity requirements that apply to electrical and electronic equipment used in residential, commercial, and light industrial environments. Within this set of specifications, there are three key high-voltage transient specifications:

- IEC 61000-4-2 [IEC6100042] – “Electrostatic discharge immunity test”.
- IEC 61000-4-4 [IEC6100044] – “Electrical fast transient/burst immunity test”.
- IEC 61000-4-5 [IEC6100045] – “Surge immunity test”.

Each specification defines a test method to assess the immunity of electronic and electrical equipment against the defined phenomenon.

The automotive industry is one of the most demanding fields in terms of reliability, and over time, it has developed its own dedicated standards to cover transients during assembly, during service, caused by passengers, or even by component switching in the machine while running.

The main standards developed to verify the robustness of vehicle systems are listed below:

- ISO 10605 [ISO10605] – “Road Vehicles - Test methods for electrical disturbances from electrostatic discharge”.
- ISO 7637-2 [ISO76372] – “Road Vehicles - Electrical disturbances from conduction and coupling - Part 2: Electrical transient conduction along supply lines only”.
- ISO 16750-2 [ISO16750] – “Road Vehicles - Environmental conditions and testing for electrical and electronic equipment - Part 2: Electrical loads”.

In addition to these standards for cars with traditional combustion engines, new methodologies have been developed for hybrid and fully electric vehicles. The most important are:

- ISO 21498-2 [ISO214982] – “Electrically propelled road vehicles. Electrical specifications and tests for voltage class B systems components”.
- ISO 7637-4 [ISO76374] – “Road Vehicles - Electrical disturbance by conduction and coupling - Part 4: Electrical transient conduction along shielded high voltage supply lines only”.

In addition to these standards, each car producer has its own amendments to the general requirements, both for traditional-engine and electric vehicles.

Moving to other fields of application, medical regulations require equipment to be in line with:

- IEC 60601-1-2 [IEC6060112] – “Medical electrical equipment - Part 1-2: General requirements for basic safety and essential performance - Collateral Standard: Electromagnetic disturbances - Requirements and tests”.

The required stresses are the same as those in IEC 61000, but the required stress levels are higher. The avionics industry operates in the most aggressive environment: the entire “system” must survive lightning strikes without disruption. The reference standard is:

- DO-160 [DO160] – “Environmental Conditions and Test Procedures for Airborne Equipment”.

This contains several sections related to materials, but also to electronics:

- Section 16 – Power input. Input power conducted emissions and susceptibility, transients, drop-outs, and hold-ups. The power input tests simulate conditions of aircraft power from before the engine starts to after landing, including emergencies.
- Section 17 – Voltage spike. This test determines whether the equipment can withstand the effects of voltage spikes on its power leads, whether AC or DC.
- Section 22 – Lightning Induced Transient Susceptibility. These test methods and procedures are provided to verify the capability of equipment to withstand a selection of test transients defined in this section, which are intended to represent the induced effects of lightning.
- Section 23 – Lightning Direct Effects. The tests described in this section are intended to determine the ability of externally mounted equipment to withstand the direct effects of a lightning strike.
- Section 25 – Electrostatic Discharge. The electrostatic discharge test applies to airborne equipment that may be subject to static electricity discharges from human contact.

Outside Sections 22 and 23, the standard refers to waveforms similar to IEC stress conditions, whereas those two sections have specific aggressors to simulate single or burst stresses.

2.4 Transient Stress Tests Defined by User

In addition to international standards, companies develop their own transient stress tests at both device and system levels based on past failures or potential aggressors identified in applications. Large companies generally provide detailed specifications; examples include GMW 3097 and 3712, DC 10614/10615, and PSA B21 7112. In these cases, suppliers have all the information needed to properly design their section of the system. In other cases, only limited information, such as a single waveform from a real application, is available. With such poor details, the risk of misunderstanding or overdesign is very high.

2.5 Documentation and Supplier/Customer Interaction

Typically, documentation of AMR values is included in the datasheet for an electronic device. Also, pass/fail results for standardized transient tests on components are included in the product datasheet or a qualification report. In the supplier-customer relationship, these documents may serve as technical and legal references for the partners' responsibilities. Also, any additional characterization is part of the customer-supplier financial negotiation.

The robustness targets of various stress tests are either given by industry-standard requirements or by the customer. The customer can decide to waive the targets if they cannot be achieved due to performance reasons. Depending on the field of application, either robustness in the automotive industry or performance and cost in the consumer market will dominate.

The datasheet plays an important role in the case of a field failure. If a component doesn't comply with the datasheet values, it can lead to a system failure in the field and make the supplier liable to the customer.

Beyond the datasheets and qualification reports, there are various technical documents, such as integration guidelines or model descriptions, intended solely for informational and support purposes in the optimized design of the system.

Chapter 3: Example of Square Pulse Testing to Determine an Acceptable Transient Stress Area of a 2-Pin Device

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Kai Esmark, Infineon Technologies

3.1 Introduction

Depending on the device type and application, different transient stress test methods or waveforms must be used to evaluate the ATSA. It is important that the transient stress condition be aligned and agreed upon between the system developer, who understands the system stress condition, and the component supplier's understanding of the IC. To visualize and exemplify the method for extracting the acceptable transient stress area, for example, for a 2-pin device, this chapter discusses a square-pulse characterization. This follows the SEED characterization concept for system ESD events. A square-pulse stress test allows easier quantitative assessment and an obvious way to integrate the total stress time of repetitive pulses. The method can address the physical mechanisms underlying both reliability and short, high-current transient pulses, including self-heating and avalanche multiplication, which can lead to immediate or latent damage (see Appendix A).

3.2 Wunsch-Bell Relation

The power-to-fail dependency for electrothermal failures of a one-dimensional system attached to an infinite heatsink is described by the Wunsch-Bell relation [Wun1968]. This has been generalized by Dwyer [Dwy1990]. To use generic terminology, the Wunsch-Bell relation will be referred to in cases where devices require 2- or 3-dimensional considerations in addition to the 1-dimensional case.

The underlying process reproduced by Wunsch-Bell is a single square-shaped current pulse that causes thermal damage due to self-heating, while accounting for heat diffusion out of the heated area. This relation allows the stress levels below and above the damage threshold to be represented by an envelope curve in a log-log plot of power-to-fail versus pulse width, as shown in Figure 5. As pulse widths shorten, there is an adiabatic region where heat diffusion can be neglected. This results in a linear relationship between power-to-fail (P2F) and pulse width. At longer pulse widths, the P2F envelope approaches a steady state in which heat diffusion balances heat generation. The steady state can be characterized by a time-independent AMR threshold for failure, whereas in the Wunsch-Bell and adiabatic regimes, a transient AMR constrains the stress pulse amplitude.

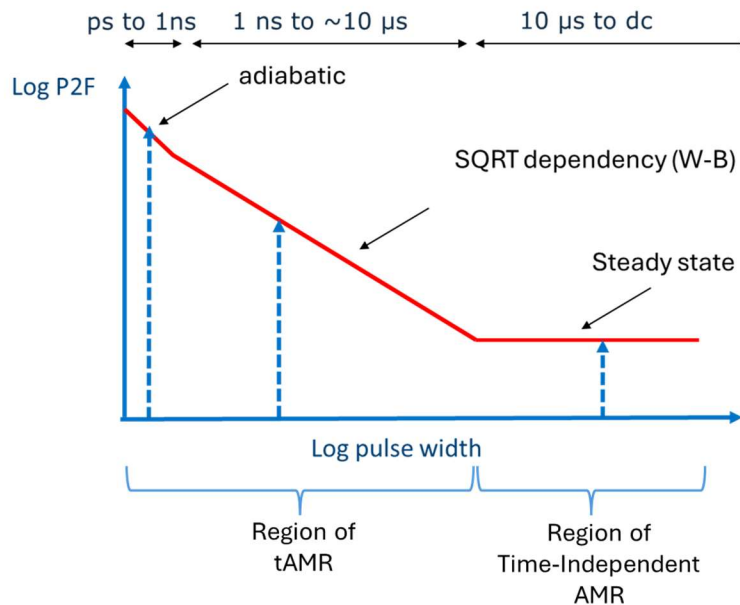


Figure 5: Wunsch-Bell Curve Describing the Power-to-Fail Dependency on Pulse Width

Note: A minimum stress level is indicated, which leads to thermal damage during the long pulse. The graph shows the P2F behavior due to electrothermal stress from square pulses with pulse widths ranging from picoseconds to seconds.

In a real-world situation, there are various limitations to this simplified concept:

- 1) Both in the real world and for standardized tests, stress pulses typically have a more complex waveform. In simpler cases, such as an HBM waveform, an equivalent 100 ns square-pulse TLP is widely accepted as reproducing the actual HBM failure level. In other cases, the pulse width of the TLP must be adjusted to reflect the thermal impact of a specific waveform; for example, a 50 ns wide TLP pulse represents the peak current of the second peak in IEC 61000-4-2 and has shown good correlation with electrothermal failures in IEC pulses [Gossner]. Another approach was adopted by [Cao2011], in which the integrated energy-to-failure is calculated for various stress times ranging from zero to the maximum stress duration. This is then compared to the failure level of square pulses of the equivalent pulse width. This can be applied to an IEC 61000-4-2 [IEC6100042] pulse, which exhibits a double-peak exponential waveform. The stress-to-fail can be calculated using a numerical technology computer-aided design (TCAD) tool for device simulation with electrothermal models.
- 2) In the case of multiple, repeated stress transients, the application of the Wunsch-Bell relation is only valid if the previous pulse doesn't affect the behavior of the device at the subsequent stress pulses.
 - a. This requires that the device reach thermal equilibrium before the next stress pulse is applied. While this depends on the system and device, it typically relaxes within a millisecond or less.
 - b. The device should not degrade at the first pulse, making it more susceptible to the second pulse. This often happens when the device is stressed near the failure threshold. To account for this, the maximum acceptable stress level needs to be derated. The

amount of derating depends on the specific technology and is commonly on the order of 10%-30%.

3.2.1 Dependency Between Electrical Stress and Reliability Degradation

Electrical stresses exceeding the MOC can degrade reliability, affecting the maximum acceptable stress level for a given lifetime. Depending on the stress and the degradation mechanism, annealing effects might counteract this. For example, in lower-level ESD stresses, it has been reported that stressing the gate dielectrics with a non-destructive ESD pulse has little impact on lifetime [III2009].

Considering these constraints, the maximum acceptable level of a stress parameter, such as current, voltage, or power, can be extracted from a Wunsch-Bell relation for short transients. For longer stress conditions, a reliability (aging) model will determine the maximum acceptable stress level (see Figure 6). The latter depends on the acceptable reduction in the lifetime (LRTS) of the device or circuit.

As the maximum acceptable stress amplitude increases with shorter pulse duration, the envelope of maximum stress shifts from a reliability-driven to an electrothermal-driven failure mode. This occurs at the minimum stress level to create thermal damage. However, at stress amplitudes slightly below this level, both effects are superimposed, and device reliability can degrade more rapidly, for example, due to self-heating or changes in transport mechanisms, such as avalanche generation.

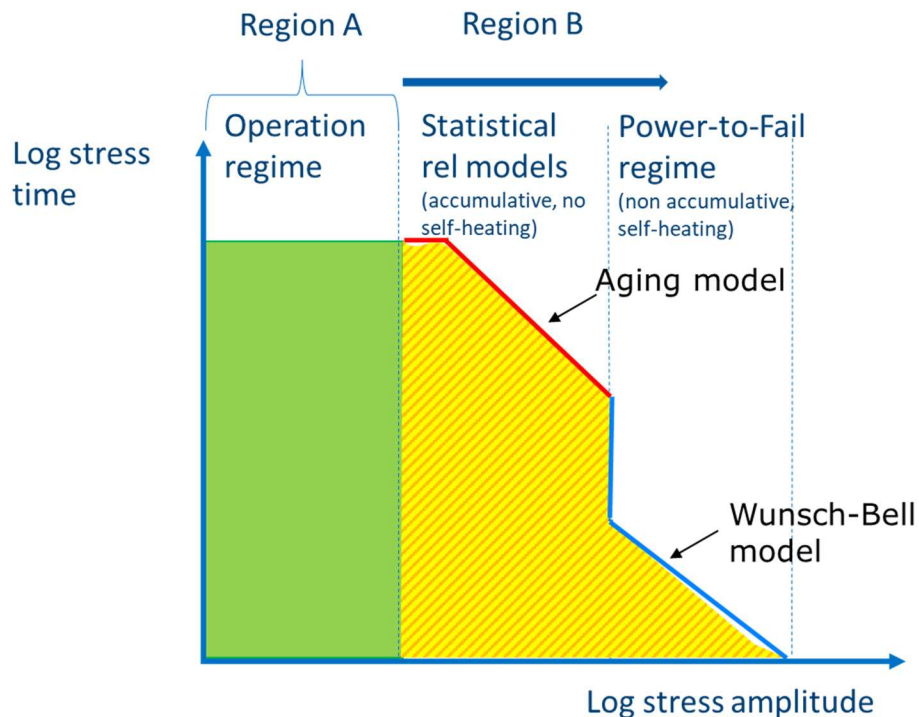


Figure 6: A Presentation of Region B in Terms of Acceptable Pulse Amplitudes and Pulse Duration Enveloped by Lifetime Degrading Reliability Mechanisms and Short Transient Thermal Fail Mechanisms (Yellow Region)

3.3 Lifetime Degradation Budgeting

To describe the concept of acceptable lifetime degradation, a differentiation between system lifetime and device lifetime is introduced. While the system lifetime is the actual operational time of the system at the end customer, which imposes minimum requirements on the lifetime of the components in the system, the device lifetime describes the potential lifetime of the devices under the given maximum operating conditions. Any transient stress beyond the device's maximum operating conditions will reduce its lifetime. To calculate a tolerable threshold for transient stress pulses, a device lifetime budget must be defined that is acceptable for the magnitude and number of transients. This is designated as a lifetime reduction for transient stress (LRTS). Figure 7 shows examples of maximum stress as a function of the acceptable reduction in device lifetime. Based on the specified acceptable lifetime reduction, an envelope of acceptable stress duration vs. stress amplitude can be determined, which divides the acceptable transient stress area from the area of premature failure. This can be applied to various degradation mechanisms, such as bias temperature instability and electromigration. The most sensitive mechanism will provide the critical limit for the circuit operation. In a properly designed system, the reduced device lifetime should be equal to or greater than the required system lifetime.

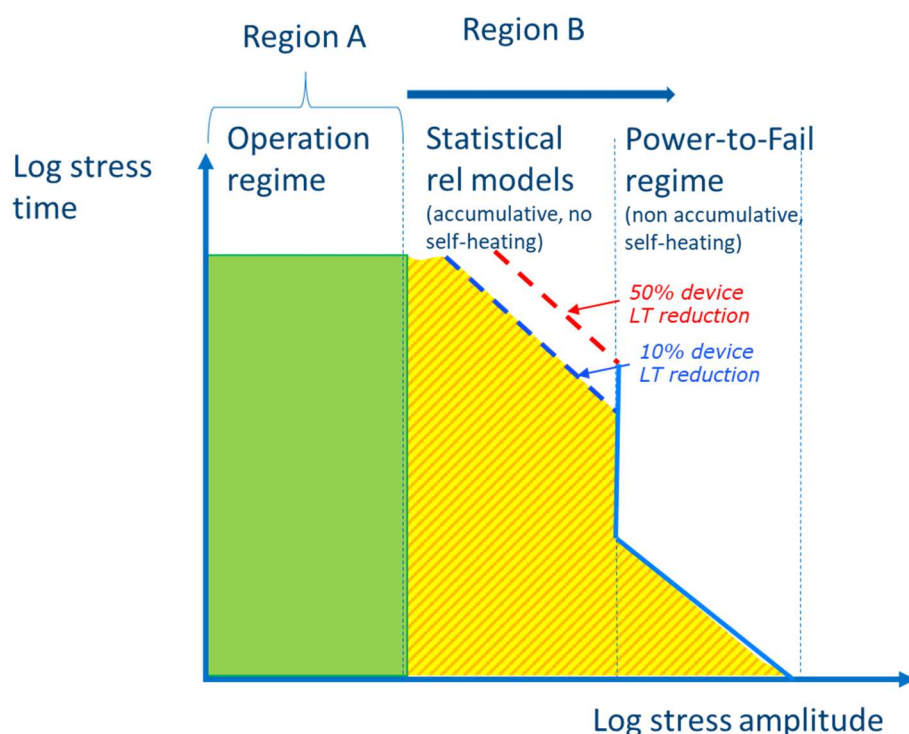


Figure 7: Envelope of Maximum Stress Levels Seen by a Device for an Accepted Lifetime Degradation of 10% and 50% of Initial Device Lifetime in the Regime of Reliability Driven Fails

3.4 Derating Methodology

To apply ATSA (introduced in Chapter 1) as design guidance for robust systems, statistical process variations and the impact of environmental and electrical parameters, such as temperature or gate voltage, need to be considered. The ATSA should be based on the worst-case operating conditions. To simplify the analysis, the results of a small-sample-size transient stress test experiment are derated (by a derating factor that creates a safety margin), which is determined by the device expert. The decision is typically based on experience with similar devices and technologies, as well as knowledge of how the circuit interacts.

The ATSA evaluation will also differ between the reliability-governed and the transient-pulse-limited regime. In the reliability regime, statistical parameters are available, and a quantitative decision can be based on 3σ or 5σ criteria. For short transients, stress testing of a few samples is typically applied. This requires expert judgment to decide on the derating criteria. Commonly, the failure level of a device under TLP stress is determined by increasing the TLP current stress in steps while measuring the device leakage after each step. An abrupt increase in leakage by more than an order of magnitude, with no observable change below this level, indicates massive, sudden damage. This is a clear indicator of the failure level. A 10%-20 % derating of the observed maximum TLP current before failure (I_{t2}) typically provides a sufficient safety margin against minor process variations. On the other hand, there are failure mechanisms that lead to progressive degradation of the junction leakage [Guitard2004]. At lower stress levels, the increased leakage is barely detectable, making it difficult to distinguish the actual failure threshold. An assessment of leakage behavior as TLP levels increase can indicate to the expert whether to explore potential degradation at lower levels, for example, through multi-zap stress.

3.5 Example of a Real-World System

The approach for determining tAMR characteristics, as discussed in the previous sections, will be demonstrated using the example shown in Figure 8. In addition, it explains how to access the corresponding data, which will help determine the tAMR limit.

A simple CMOS circuit is analyzed. The sensor product only contains supply and GND pins. The signaling of the IC happens through the supply pin. In parallel with the functional part, there is a protection element designed to protect the functional unit within the specification of the product. The device must be robust against transient stress conditions appearing in the application.

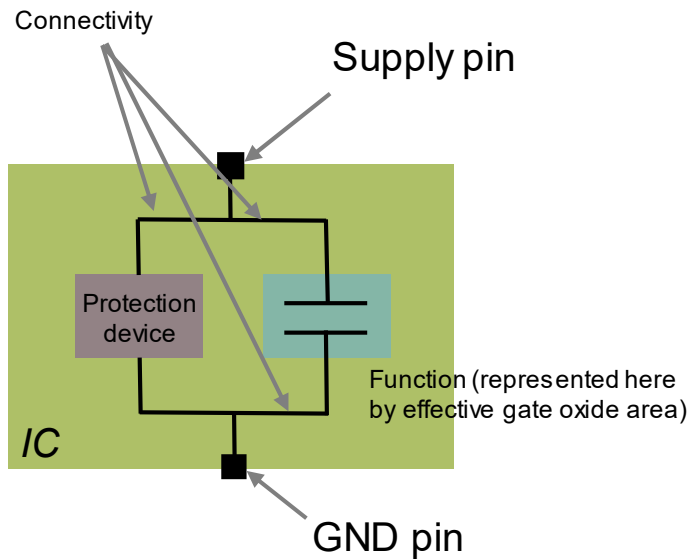


Figure 8: Assumption of a Simplified Product Architecture to Determine the tAMR Limit
Note: The IC consists of functional units, an associated protection element, and metallic interconnects (either on the package or die level).

The process technology includes MOS devices operating at a nominal gate voltage of 3.3 volts. To determine the tAMR of the product, we need to analyze the robustness of both the functional unit and the protection element. The functional unit is simplified and represented by a gate oxide capacitor.

Properties of the Protection Element: An ESD protection element is characterized by the fact that it switches to a low-ohmic state. In this state, they efficiently shunt current to ground, thereby sustaining the electrical stress and limiting the clamping voltage at its external terminals to a sufficiently low value. Once activated, the protection element typically exhibits significant self-heating during the transient stress pulse. Excessive self-heating can damage the protection element. Beyond a threshold level, thermal destruction of the ESD protection element will be the dominating failure mechanism.

Properties of the "GOX" Device: The voltage dependence of the gate oxide lifetime in the underlying process technology is usually described by a power law. Fundamental parameters such as the maximum gate oxide area and/or the gate oxide thickness are included in the calculation. The calculation also considers temperature dependence and the acceptable failure-in-time (FIT) rate. The result of the calculation, based on the power law, is the remaining lifetime after a given voltage stress is applied to the gate oxide. It is assumed that the remaining lifetime depends only on the stress voltage (not on current or power).

The graphs in Figures 9 through 11 can be derived from TLP measurements of pulses with various durations on the gate oxide and the protection element.

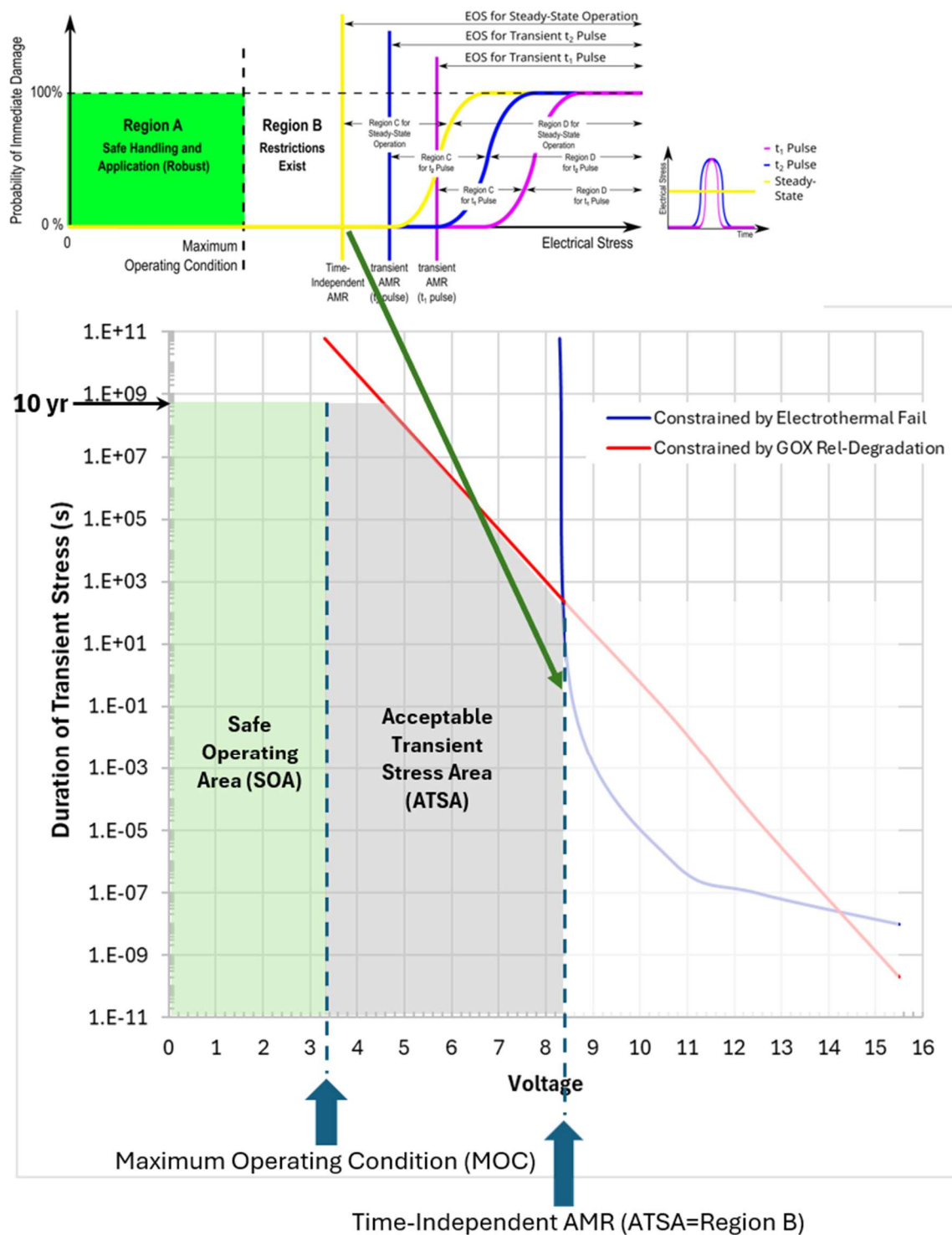


Figure 9: Reliability/AMR Limits of a 3V3 Interface Containing an ESD Protection Element and a Gate Oxide (GOX) Structure for a Time-Independent AMR (e.g., > 1 second)

Note: The green area represents the region of safe operation with a guaranteed lifetime, while the grey area indicates the regime of acceptable transient stress, tolerating a certain degradation of lifetime.

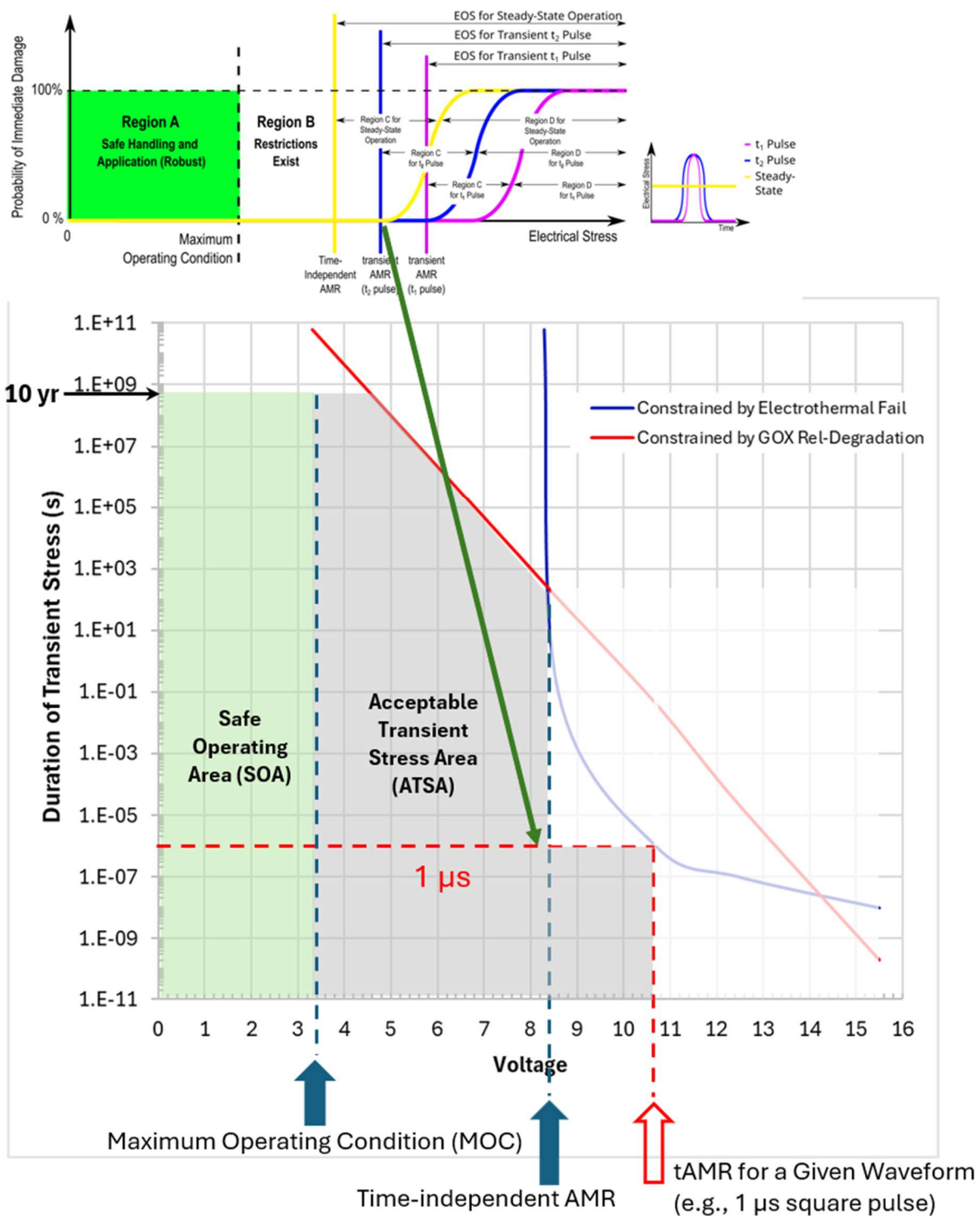


Figure 10: Reliability/AMR/tAMR Limits of a 3V3 Interface Containing an ESD Protection Element and a Gate Oxide (GOX) Structure for a 1 µs Square Pulse

Note: The green area represents the region of safe operation with a guaranteed lifetime, while the grey area indicates the regime of acceptable transient stress, tolerating a certain degradation of lifetime.

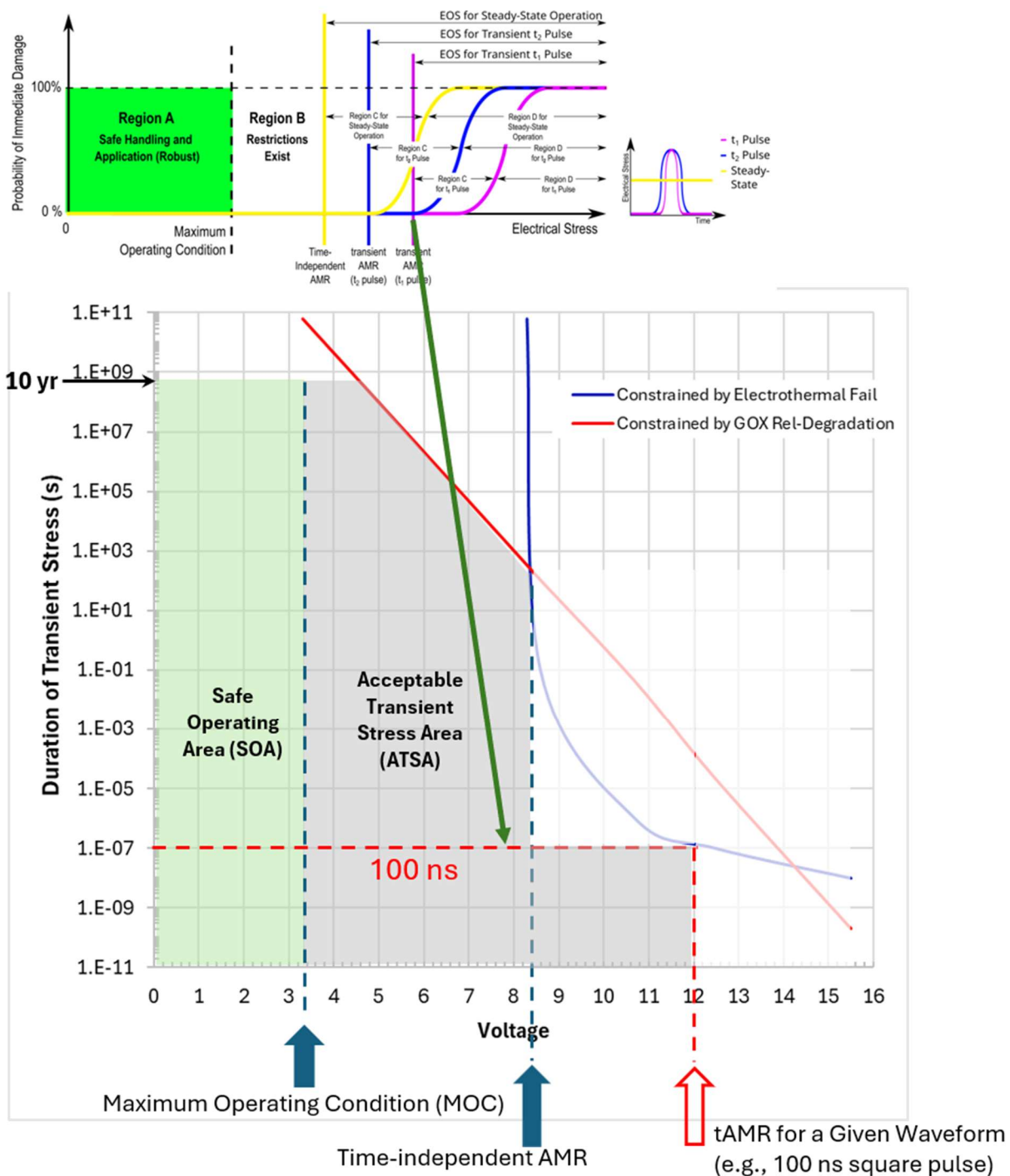


Figure 11: Reliability/AMR/tAMR Limits of a 3V3 Interface Containing an ESD Protection Element and a Gate Oxide (GOX) Structure for a 100 ns Square Pulse

Note: The green area represents the region of safe operation with a guaranteed lifetime, while the grey area indicates the regime of acceptable transient stress, tolerating a certain degradation of lifetime.

By specifying the magnitude of the voltage stress, the maximum stress time for the protection element and gate oxide can be extracted. The plot was created by assuming an initial lifetime (10 years) due to the stress. In a simplistic view, the device will fail above the 10-year line. Alternatively, lower lifetime degradation can be considered, as shown in Figure 7.

As long as the system's maximum operating conditions are never exceeded, it is guaranteed to last 10 years. However, if voltage transients exceed 3.3 volts in the system, the device's lifetime will decrease. If a lifetime reduction for transient stress (LRTS) is defined, the maximum stress pulse voltage can be extracted for a given pulse duration (red line in Figure 9). In a region where the voltage remains below the ESD element's trigger voltage of 8 volts, as in the example, the reduction in sustaining time is governed solely by the gate oxide degradation mechanism.

Beyond the voltage at which the ESD element can also be thermally damaged (in this case, the shunt element has an activation voltage of 8 volts), the protection element's stress-to-fail threshold must also be considered. In this region, the ESD element experiences thermal damage, whereas the gate oxide alone would allow higher voltages. The ESD element now represents the weakest link. The situation reverses at higher voltages (approximately 14.2 volts in this case).

As shown in Figure 9, an acceptable transient stress area is defined by the reliability-constrained line (red line) and the limit at which the ESD protection element first experiences thermal damage. If this crossover occurs in the steady-state region of the stress-to-fail characteristics (see Figure 5), the limit is defined by the time-independent AMR at 8.2 volts.

The ATSA region can be extended for given waveforms (here: square pulses of defined pulse duration). In Figure 10, an additional region of ATSA has been extracted for a 1 μ s (and shorter) square pulse reaching 10.6 volts. This value is indicated as the tAMR level for this specific waveform. For shorter pulses, this increases the ATSA area, as shown in Figure 11 for a 100 ns TLP, where the tAMR value is 12 volts. **To define a practical, acceptable transient stress area for short stress transients as a specification for system design, process variations, statistical effects, etc., need to be considered. The ATSA and tAMR parameters are then solely defined by the IC supplier based on the stress waveform provided by the system customer.**

A number of influencing factors have been simplified or disregarded in the discussion above:

- Interaction between the activity of the protection element and the functional part of the IC has been neglected. For example, heat generated during activity in the protection element also spreads to the functional areas of the IC and can lead to greater gate oxide degradation.
- Other reliability degradation mechanisms like aging of the interconnects on the chip or in the package by electromigration are neglected; for example, this can be critical in situations of high inrush conditions.
- No multi-zap effects occur that reduce the value of the voltage at which damage to the protection element is triggered (V_{t2}).
- A square wave may not be a reasonable approximation of the stress. More complex waveforms need to be approximated by various step-type pulse shapes, and the combined effect of the degradation needs to be extracted.
- Application of the power-law characteristics to the condition of the gate oxide in the ESD time domain may not be correct. The extrapolation of the lifetime power-law of gate oxides into the ESD time domain typically leads to a pessimistic gate oxide breakdown value, which, in our case, results in another crossing of the two characteristics at around 14 volts, as shown in Figures 9-11. This would mean that during a CDM stress (<1 ns), the weakest link is again the gate oxide. Characterization of gate oxide breakdown using short pulses

is more accurate. Additionally, effective ESD protection ensures that the gate oxide breakdown voltage is not exceeded during pulses in the nanosecond to several-hundred-nanosecond regime.

As technologies advance and gate oxides get thinner, the power law for gate oxide lifetime will shift to the left, as shown in Figure 12. There could be a situation in which the gate oxide lifetime is shorter than the thermal lifetime across the full voltage range. This emphasizes the need for more effective protection elements with improved voltage clamping capabilities in advanced technologies.

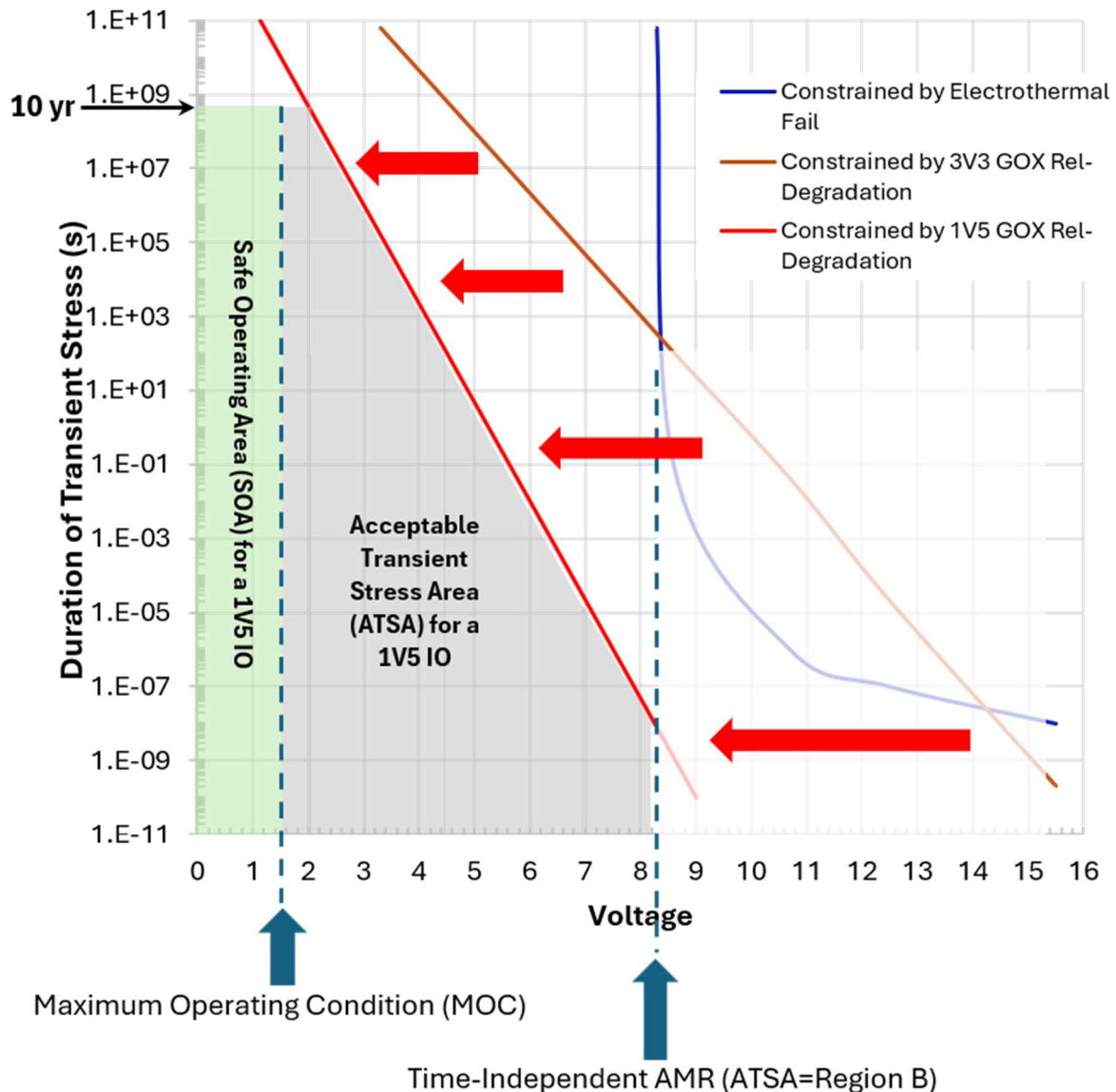


Figure 12: Change in Power Law Behavior When Switching to Technologies with Thinner Gate Oxide Thicknesses
Note: Here, the transition is from a 3V3 node to a 1V5 node (for illustration purposes only; the protection device remains unchanged). As a result, the ATSA region shrinks and is now entirely dominated by the robustness condition of the 1V5 GOX used in the IO.

Chapter 4: Summary

This white paper has introduced the following aspects to the discussion of tAMR:

- 1) A terminology (ATSA, LRTS, and tAMR) and a definition of terms to facilitate communication between component suppliers and system designers to support the development of robust systems.
- 2) Application of tAMR concepts typically occurs in one of two main scenarios:
 - Pre-design/ideal planning stage, where, early in the process, the customer provides definitions of aggressor pulses that the IC should be able to survive, allowing the component supplier to proactively design the device to handle them. This is the desired and most reasonable approach
 - Post-analysis or field-failure “catch-up” mode, where the customer presents a new, unexpected pulse and requests reliability certification, often superimposed on a running product cycle where new pulse requirements identified in the field become desirable for next-generation designs.
- 3) ATSA and tAMR are parameters solely defined by the IC supplier based on the stress waveform provided by the system customer.
- 4) Various examples of transient stress conditions covered and not covered by typical standards have been presented as a reference for discussion in the industry.
- 5) The failure signatures in terms of the underlying physical phenomena of thermal damage and dielectric degradation/breakdown have been highlighted. Based on the example of a simple two-pin device, a square-pulse characterization of tAMR has been presented to illustrate aspects of reliability degradation, thermal damage, and the acceptable transient stress area (ATSA).

Appendix A: Relation of Transient Stress and Reliability Degradation

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A.1 Introduction

A fundamental topic in assessing the impact of stress on a semiconductor component is understanding the underlying physical mechanism. The assessment can be driven by two different motivations:

- 1) addressing the root cause
- 2) addressing the effect

Depending on the purpose, very different approaches will be taken for the assessment. Commonly, the failure location is determined through physical failure analysis, which determines the type of failure, such as metal melting or rupture of a gate oxide. Knowing (or guessing) the entry point of the stress and the general type of stress, in terms of waveform and amplitude, allows reconstruction of the stress path and the critical device parameters that lead to the observed failures. This can also be reproduced by simulation and replicated under a well-controlled electrical stress, such as TLP injection, though any correlation with real-world electrical stress events is not guaranteed. This ultimately leads to the conclusion that the real-world stress and failure mechanisms can be immediate thermal damage, dielectric breakdown, electromigration, or some other degradation mechanisms.

In system design optimization, the failure mechanism and the associated critical stress threshold serve as the starting point for the assessment. The design measures are rated based on their ability to mitigate stress at the most critical location in the system. An important method for this assessment is simulating the device and circuit behavior of the IC and the printed circuit board (PCB), as well as the electromagnetic behavior of the system.

A.2 Failure Mechanisms

A.2.1 The Variety of Failure Mechanisms Possible on a Single Pin

Failure mechanisms in semiconductor devices are summarized in JEDEC publication JEP122 [JEP122], which also lists many other documents that provide further information and models for each mechanism. We will focus here on specific failure mechanisms related to EOS and electrical stress that exceed the physical capabilities of the materials involved. Physics of failure analysis reveals 3 basic causes of physical damage from EOS: thermal, electric field, and electromigration. These are discussed in further detail in the next sections. Figure A1 is a conceptual example of an IO pad with an ESD protection circuit. When an electrical stress interacts with a package-exposed pin, the stress will find the "weakest link". The weakest link may be in the ESD protection circuit or in the core circuit elements if the stress gets past the ESD protection.

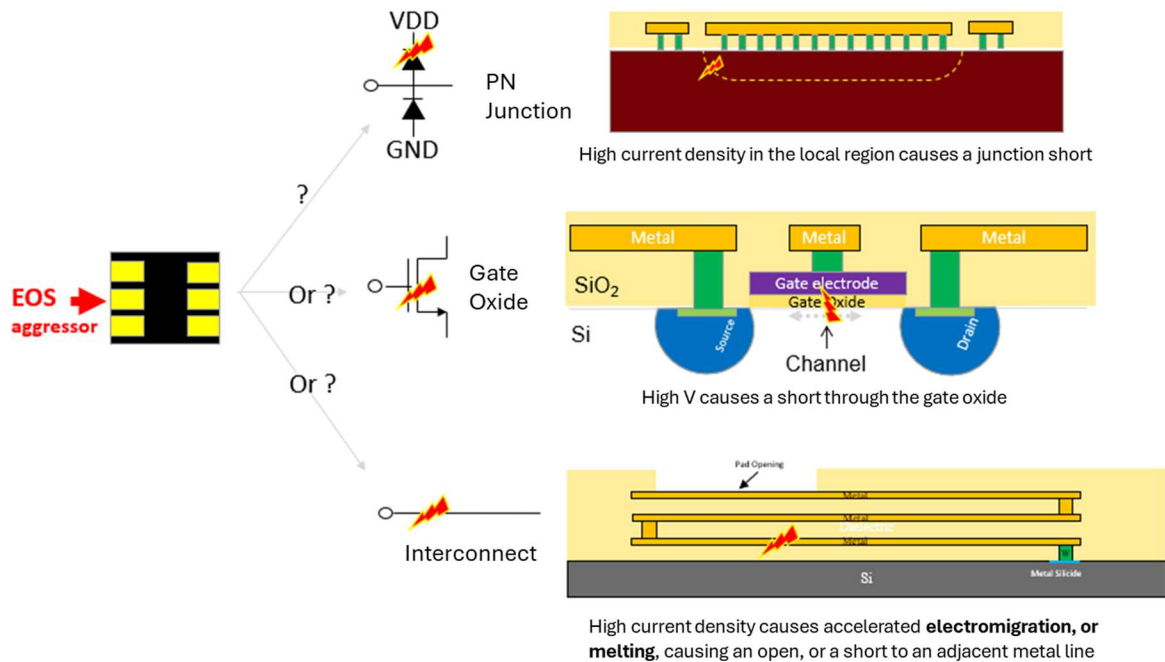


Figure A1: Pictorial Representation of Potential Failure Mechanisms Caused by an EOS Pulse [courtesy Stevan Hunter]

The numerous possible outcomes depend on multiple factors. In Figure A1, the stress on the pin may cause thermal damage to a semiconductor junction, the electric field may cause a dielectric rupture, or a high current density may accelerate electromigration in the interconnect metal. In addition, latch-up may occur, depending upon many factors. Once triggered, a failure often leads to further damage and thermal issues in the circuitry, especially if the electrical stress persists for an extended period or is repeated.

A system manufacturer that wants to warrant certain transients beyond the published AMR without causing EOS damage will need to make a substantial effort to characterize the product pin by pin for each aggressor pulse of interest. This would involve determining the failure mechanism and threshold for the weakest element, followed by the appropriate reliability stress testing to investigate potential latent damage, and then applying an appropriate derating factor. Unless a significant payback is expected, the authors of this white paper generally agree that system manufacturers are unwilling to incur this extra cost and incorporate it into their product development and qualification practices, because a system manufacturer's focus remains on product characterization and qualification within published operating limits.

Operation beyond the maximum operating condition (MOC) will accelerate wear-out mechanisms. Considering the potential effects of transient EOS "slightly beyond AMR" on circuit elements, physical damage will accelerate wear-out. Electromigration, time-dependent dielectric breakdown, and semiconductor junction degradation are all considered wear-out mechanisms that can be predicted using mathematical models. Latch-up could also be triggered "slightly beyond AMR". These mechanisms will be discussed first, followed by other possible failure mechanisms initiated by EOS. EOS "well beyond AMR" is more likely to cause immediate failure, latch-up, or initiate a new failure mechanism with either latent or immediate damage.

A.2.1.1 Electromigration (EM)

Electrical current is distributed on the surface of metal conductors and occurs through the bulk material in microscopic interconnects. Electromigration (EM) is the process whereby the electron current flow imparts momentum to metal atoms, causing them to physically migrate in the same direction (opposite to the conventional current flow). Damage begins with the accumulation of metal atom vacancies, increasing electrical resistance in narrow conductors. A failure occurs when resistance increases out of spec, and if still powered, we expect an electrical open shortly thereafter, caused by a void in the interconnect near the anode. A failure may also occur due to an electrical short from a hillock or extrusion of the metal due to a pileup of migrated atoms at the cathode. EM is controlled by the interaction between the electrical current density and the characteristics of the metal itself, such as grain size and orientation, as well as the presence and distribution of alloy or contaminant atoms. Metal atoms electro-migrate more easily at higher temperatures, leading to earlier failure.

High current flow promotes accelerated electromigration by raising local temperature, rapidly leading to voids and melting. Copper (Cu) and aluminum are the most common metallization in ICs, with Cu being more robust against EM. Film deposition conditions, annealing process, and barrier metals are incorporated to optimize metal interconnect robustness against EM, but even the Cu metallization, being so thin and narrow, with non-symmetrical interfaces between layers and a lack of room for redundant structures, is pushed to its very limits. AMR, set to preserve the reliability of metal interconnects, should be considered a serious limit to reliability, especially with 8, 10, or 12 layers of interconnect on ICs. Intermittent performance or permanent interconnect failure on a chip with billions of interconnect elements can ruin performance and perhaps take the system down.

A.2.1.2 Transients and EM

It may be that metal interconnects can tolerate some level of transients involving only tiny currents, because electromigration is worse at high current density, though damage accumulates as voiding. However, metal interconnects are not the only elements to be protected. An aggressor pulse that may have only a slight adverse effect on the metal could still damage a dielectric.

A.2.1.3 EM as “Weak Link”

EM may be designed to be the earliest or weakest wear-out mechanism in an IC, with all other failure mechanisms predicted to last longer under *in-use conditions*. Strict design rules are in place to ensure the reliability of properly manufactured products by prohibiting excessively narrow lines, spaces, or film thicknesses. If this is the case, then AMR may focus on the maximum current density tolerated by interconnects, appropriately derating based on statistical considerations and maintaining an adequate margin to protect reliability.

A.2.2 Semiconductor Junctions

Semiconductor junctions rarely tend to “suddenly burn out” during operation unless through some latch-up event. Instead, they may gradually degrade in performance, with failure due to a parameter (leakage) eventually drifting out of spec. The operation of the circuit above AMR is expected to accelerate wear-out through subtle damage. As the voltage above AMR increases, the junction may experience avalanche breakdown. Junctions may be damaged by fast-rise-time aggressor pulses, causing high current flow to concentrate in a microscopic region, leading to thermal

runaway and melting (see the Wunsch-Bell curve discussion below). The weakest element may be the p-n junction connected to the input, DC power supply, or output terminal. P-n junction burnout failures occur when the temperature reaches the approximate melting point of silicon—thermal overstress. Repeated static pulses at voltages below a certain level cause no damage to the p-n junction, indicating that there is a clearly defined failure threshold. ESD can cause this type of junction damage, especially CDM, due to the extremely fast rise time of high-current pulses. Advanced technology nodes have junctions that are much less robust against ESD and are increasingly sensitive to operation beyond MOC and EOS beyond AMR.

A.2.3 Time Dependent Dielectric Breakdown (TDDB)

TDDB is described as a dielectric failure caused by a conductive path forming in the dielectric over time under constant low stress. TDDB is not the same as the dielectric breakdown voltage, V_{bd} , at which the electric field across the dielectric exceeds its dielectric strength, causing immediate failure. TDDB has a lower voltage compared to V_{bd} , and the failure of the dielectric film is due to having a sustained electric field over time, eventually accumulating charges into a leakage path for “soft breakdown”, which can develop into a permanent failure. The same electric field that caused the breakdown drives current through the dielectric at a microscopic level. As current flows, local temperature increases, causing increased current flow, thermal runaway, melting, and a permanent short circuit. TDDB in the gate oxide of a MOSFET ruins the device's performance.

A high-quality oxide in the device is designed to perform well throughout the full warranty period. Eventually, in continued stress, the dielectric will suddenly break down. TDDB is considered a wear-out mechanism, as it is time- and electric-field-dependent. Failures occur randomly and suddenly under continuous voltage stress; the “wear-out time” depends on the dielectric characteristics and thickness, temperature, and the electric field across the dielectric. TDDB is well characterized for the intrinsic dielectric before product development, so designers know how to design reliable devices. MOC for voltage is carefully set to ensure that thin dielectrics are not overstressed in use and do not become the “weak link” in wear-out, while providing the best possible functionality for the product.

The EOS effect on dielectric integrity causes early dielectric breakdown. Latent damage is unlikely in the TDDB mechanism unless the number of EOS events over the lifetime of the device is high. AMR considers TDDB wear-out modeling, limiting both voltage and product use time to ensure reliable performance of millions or billions of transistors in the IC, all of which may use the same dielectric material. Sustained voltage above MOC will result in earlier dielectric wearout, and, beyond AMR, will eventually reach the breakdown voltage, causing immediate destruction. Transient voltages above the AMR could cause latent dielectric failure or an immediate, permanent breakdown, especially if above V_{bd} .

The thin gate dielectric of core MOSFETs is susceptible to breakdown at very low voltages. ESD and many other types of EOS could very easily damage core elements with the thin dielectric. ESD protection circuitry is placed on ICs between the outside pins and core circuitry to protect against specific ESD events in the unpowered state, namely HBM (up to its published withstand voltage) and CDM (up to its published withstand voltage). But EOS is by no means limited to these particular events. The common occurrence of gate oxide failures in customer returns indicates that EOS is reaching the core, though the specific EOS event is rarely identified. If manufacturers or

customers knew exactly which EOS events would occur, they could implement mitigations to prevent failures. In the absence of such knowledge, manufacturers simply publish AMR to warn customers that EOS must be controlled below these levels to preserve reliability.

A.2.4 Latch-up

Latch-up can be triggered by a high voltage or current, often not far beyond AMR, resulting in the *turn-on* of coupled parasitic bipolar transistors and creating a low-impedance path between power and ground *that does not turn off until power is removed*. Once triggered, latch-up can cause device failure due to excessive current flow, leading to thermal runaway. Latch-up robustness and snapback voltage (V_{t1}) are specifically tested during product qualification, providing important data to help the manufacturer set AMR. Customers who suspect that AMR is set arbitrarily low should consider that “tighter” absolute maximum limits may be necessary due to specific latch-up concerns. Latch-up robustness can in fact be considered a tAMR limit (if applied with realistic durations).

A.2.5 Dielectric Films, Capacitors

EOS damage to dielectrics may be characterized as immediate, as it doesn’t begin with small or latent damage but simply “breaks” when overstressed. Every dielectric film has a breakdown voltage, V_{bd} , the voltage at which the electric field stress exceeds the material’s capability. Voltage above V_{bd} will cause a leakage path to form, resulting in a short circuit through an avalanche process that can melt the material.

A temporary or “soft” breakdown can occur when a voltage transient is only slightly high and of short duration, with the breakdown recoverable after the electric field is removed. Don’t confuse dielectric breakdown due to EOS voltage with dielectric TDDB, which is a dielectric wear-out mechanism.

Low-K and e-low-K materials used as inter- and intra-metal dielectrics exhibit lower thermal conductivity, increasing ESD sensitivity. Withstand voltages for ESD and AMR values take these sensitivities into account.

A.2.6 Stress Voiding in Metal Interconnects

Stress voiding is driven by a mismatch in the thermal coefficient of expansion between materials. Temperature cycling encourages the growth of voids, which are open regions within the conductor, thereby increasing resistance and reducing thermal conduction. Temperature can be generated by current flow, causing local heating; therefore, the IC design must mitigate it through design rules. The AMR is intended to slow the formation of stress voids so they won’t become a reliability problem. EOS does not directly affect stress-void growth but can influence voiding through temperature excursions.

A.2.7 Extrinsic Failure Mechanisms

Semiconductor product failure mechanisms such as bond wire fusing, solder ball fatigue, and EM are typically less sensitive than the elements within the IC, so adhering to AMR also preserves the reliability of the assembly and packaging elements. Reliability qualification testing stresses extrinsic failure mechanisms to validate that none are triggered when the limits are adhered to. Customer returns having fused-bond wire, evidence of melted solder, and “burn holes” in the

package; have experienced large energy EOS events, probably well beyond AMR. Refining AMR values or embellishing AMR to allow certain transients slightly above existing limits will not help prevent high-energy EOS events.

A.3 Impact of Transient Pulses on ESD Protection and Beyond

An ESD event with a high voltage but a small charge is intended to be diverted by the ESD protection circuitry on that pin. An ESD event, such as a charged board event (CBE) with a large quantity of charge, could easily deliver enough energy to damage the ESD protection circuit. Methods for damaging circuitry in an IC by an uncontrolled stress are unlimited. So manufacturers provide an AMR to alert customers of the limits.

ESD protection circuitry is designed *not* to respond to regular signals, as this would degrade normal circuit performance. Given the infinite variety of electrical stresses, ESD protection circuitry may or may not be the victim, and if not, the core circuitry can be. Do not mistakenly assume that ESD protection circuitry also protects against any electrical stress. The behavior of the ESD protection circuitry and the damage that occurs depend on the type of electrical stress and the type of ESD protection circuitry. There are two types to consider, as discussed below.

A.3.1 Circuit-to-ESD Influence

This type of influence on internal/core circuits is caused by the ESD circuit (switch) triggering. Ideally, an ESD structure that is off during normal operation is immune to desired signals and responds efficiently to undesired ESD/other pulses. Displacement current is created by significant variation in input voltage (dV/dt) signals and substantial variation in incoming current signals (dI/dt). Switching and early triggering (mis-triggering) of ESD networks can interrupt circuit behavior.

The triggering voltage (V_{tl}) of a dynamically-triggered ESD structure is altered by the pulse rise time (t_r). The dependence of V_{tl} (trigger voltage) on t_r (rise time) is called the $V_{tl} \sim t_r$ effect. The degree of dependence varies with the type of ESD structure. One design challenge is to create triggering mechanisms that are immune to dV/dt or dI/dt effects, or that respond to transients within the correct dV/dt or dI/dt range.

A.3.2 ESD-to-Circuit Influence

This is a scenario in which ESD-induced parasitics include resistor-capacitor (RC) network delay (CESD, RESD), substrate noise coupling, and ESD self-generated noise. The design challenge for this type of influence is to reduce parasitic (off-state during normal operation) capacitive effects (CESD).

A.4 Relevance of Simulation

There are different simulation models (lumped models, real circuit-level models, TCAD, etc.), each dependent on a multitude of factors, such as data availability, analysis requirements, and time. Simulation methodologies can provide valuable assistance in analyzing and understanding the transient stresses and failure mechanisms. Further, simulation can narrow the focus area by identifying regions of interest on the chip/system and transient waveforms of interest. These

insights can be highly useful in designing more robust systems. Modern simulation frameworks can also leverage distributed computing in the cloud and newer machine learning (ML) techniques to improve the runtime and capacity. The simulation techniques relevant here can be broadly divided as follows:

1. System simulation
2. Circuit simulation
3. Device simulation
4. Novel simulation techniques (for example, ML, reduced order modeling, etc.)

Before we look into various simulation methods, it is worthwhile to briefly understand how simulation can assist with root cause analysis and design impacts.

A.4.1 Circuit-Level Simulation

Circuit-level simulation can help with root cause analysis when a user experiences a component failure, and a simulation can be used to verify or identify the failure location. In this case, the simulation setup and the models must be highly accurate to reliably capture the failure location. In many cases, the root cause cannot be inferred from the simulation results because the simulation models do not capture all the physics. The user may need to run a simulation in several steps, from the system level down to the device level, for root cause analysis.

A.4.2 System-Level Simulation

A system-level simulation typically involves models of the chip, package, and system. An example framework is shown in Figure A2.

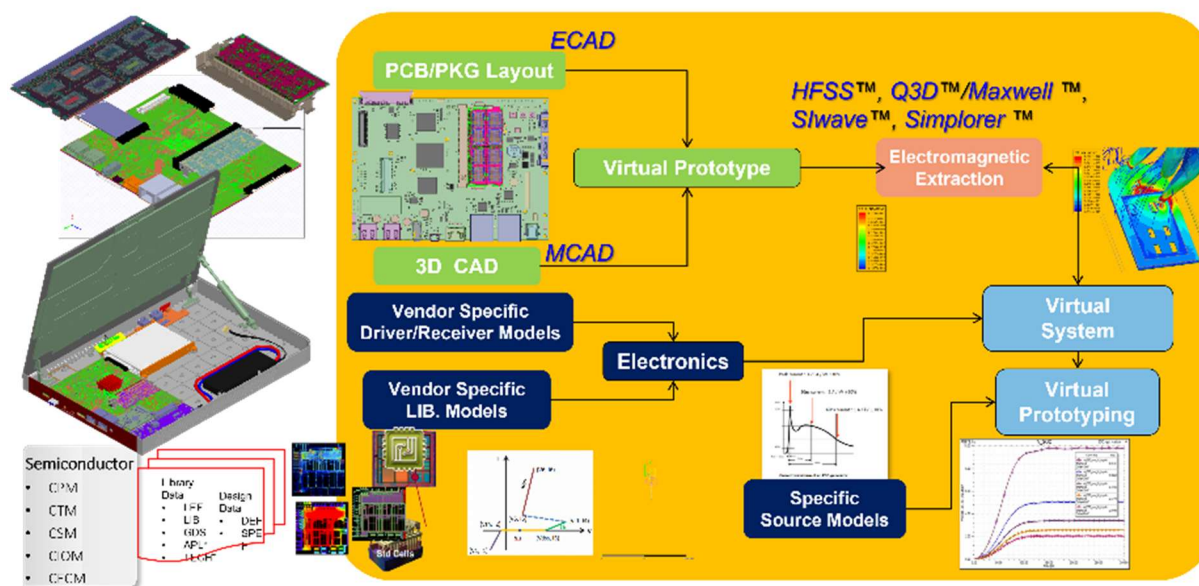


Figure A2: Example Framework for System-Level Simulation

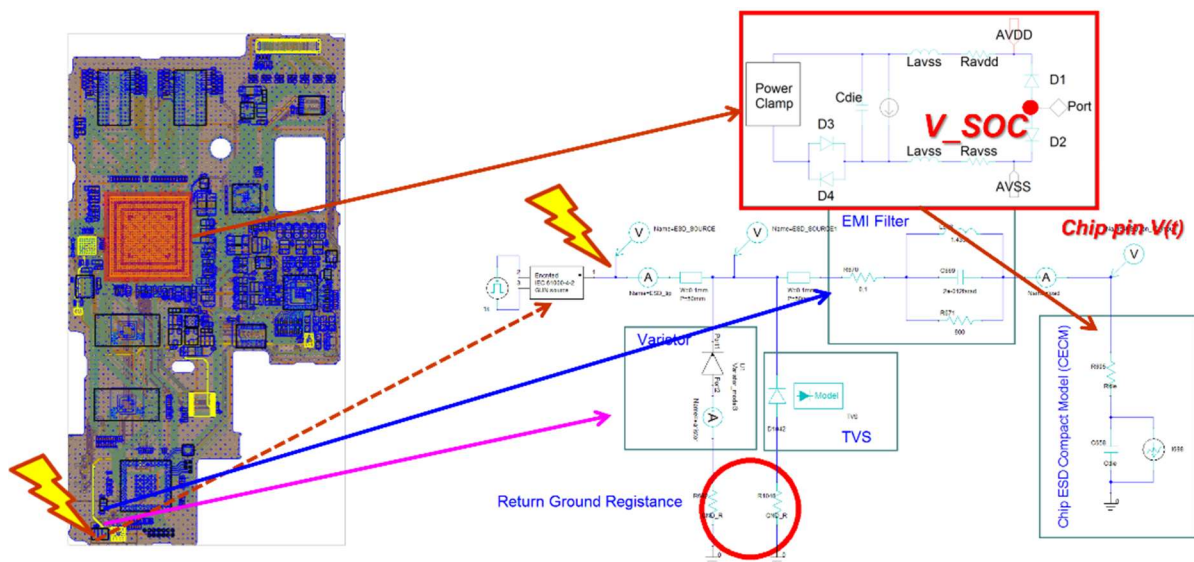


Figure A3: System-Level Transient Propagation Modeling Example

The main components of a system-level simulation are detailed PCB/package (PKG) models and an abstract chip model. Of course, generating these models requires several inputs, some of which are shown in Figure A3, which illustrates the various tools involved in this process. To determine the system's electrical properties, a 3D computer-aided design (CAD) tool may be necessary. Electromagnetic extraction tools can then be used to obtain the electrical parameters describing the PCB planes, traces, and vias. Additionally, we require models for various protection devices, such as TVS diodes, ESD filters, etc. These device models can be SPICE models, behavioral models (such as VHDL-AMS for a TVS diode), or full 3D finite element method (FEM) models (such as those for ESD filters). The resulting electrical model is then combined with a simplified and abstracted compact chip model.

The abstracted compact chip model should include compact models for on-chip parasitics, current signature models for the ports for the given simulation, and, optionally, models for on-chip protection devices such as RC-clamps/GGNMOS/diodes. In a simple case, the model can be a single lumped RC model. The passive model should include all the on-chip coupled capacitances, the decoupling capacitance, and the load capacitances. Additionally, the die model must be accurate in the gigahertz range, since a transient generally has a broad spectrum. This simplified lumped-electrical model of the chip is connected to the PCB/PKG electrical model to form the complete chip-package-system model. To simulate transient propagation in this system-level model, a transient source model is required to apply the necessary transients. Figure A4 shows an example of a transient propagating from a pad to the chip's ports, along with models of the various protection devices. A SPICE-like simulator can be used to simulate the behavior of a transient propagating through the chip package system. Using this model can help in understanding and analyzing system behavior at various locations on the PCB/PKG and in capturing the shape of the transient at the ports of the compact chip model.

A.4.3 Circuit/IP Level Simulation

In the simplest case, the circuit-level simulation can be a netlist of the desired portion of the chip without parasitics, with the transient applied to the specified pin of the chip captured from the

system-level simulation. This netlist can include transient-simulation models, such as Berkeley short-channel insulated-gate field-effect transistor models, for the devices. These device models, however, are meant for functional simulation and behave well within the devices' normal operating regions. Simulation behavior will be unreliable outside the device's operating regions and will often lead to convergence issues. Additionally, these simulation frameworks cannot handle the snapback behavior of the protection devices. Therefore, this simple transient analysis can at best provide a qualitative assessment of the transient's impact on the devices. Including the parasitics can make the simulation a little more realistic.

An example simulation framework for comprehensively handling the various scenarios is shown in Figure A4.

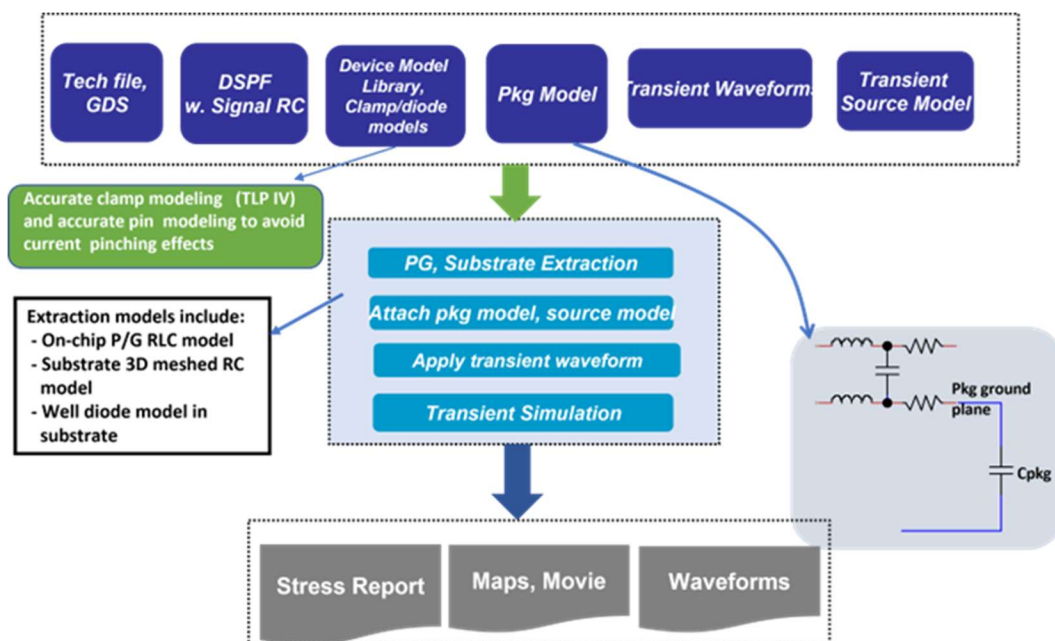


Figure A4: A Circuit/IP Level Simulation Framework for Transient Simulation

The simulation framework shown here improves upon the basic circuit simulation by adding several details. These details include the parasitics, including the substrate models, modified device models, which can achieve more reliable simulation convergence when operating outside the device's normal operating range, and clamp/diode models, including the snapback behavior. At this stage, we can optionally include either a simplified lumped RLCK package model or a fully distributed RLCK package model. While running the analysis, parasitics of the signal nets of interest can be obtained from a file, such as a detailed standard parasitic format, and the power-ground nets of interest can also be extracted. The substrate network will also impact the behavior of the transient propagation through the circuit and the stresses on the devices. A detailed 3D resistor mesh, along with PN-junction diode models, can be included in the simulation. The limitation of this approach is the number of devices that can be simulated. With an enhanced high-capacity simulator, this approach can enable simulating a netlist with millions of devices. Therefore, for this type of circuit simulation, the user can identify areas of interest on the chip and include elements only from the limited areas.

A.4.4 Device Simulation

Device simulation, such as TCAD, can be used to understand a device's behavior with high accuracy. However, it requires detailed device modeling, which may not always be available. At a broad level, device simulation requires 3D device geometries and doping concentrations. The device simulator then creates a mesh on the device geometry for numerical calculations. The finer the mesh, the higher the accuracy. The boundary conditions on the created mesh are applied, and the differential equations, such as Poisson's equation and transport equations, are solved numerically until convergence. The results of such a simulation will show the detailed potential gradient across the geometry and the device's voltage-current characteristics.

A.4.5 Novel Techniques

It may be worthwhile to mention that newer techniques in algorithms and software design, such as machine learning (ML) and cloud-based distributed computing, can greatly assist with simulation, either end-to-end or by addressing parts of the simulation problem. Examples of such research efforts are [Xiong2018], [Rosenbaum2020], and [Kumar2020].

A.4.6 Conclusion: Value of Simulation

Simulation tools and flows can provide valuable assistance in an analysis by providing qualitative and quantitative results. Although modeling the physics of a tAMR failure threshold is a difficult problem, the current generation of simulation tools can be leveraged to provide insights into both root cause analysis and design optimization. An example flow demonstrating the simulation-assisted physical testing is shown in Figure A5.

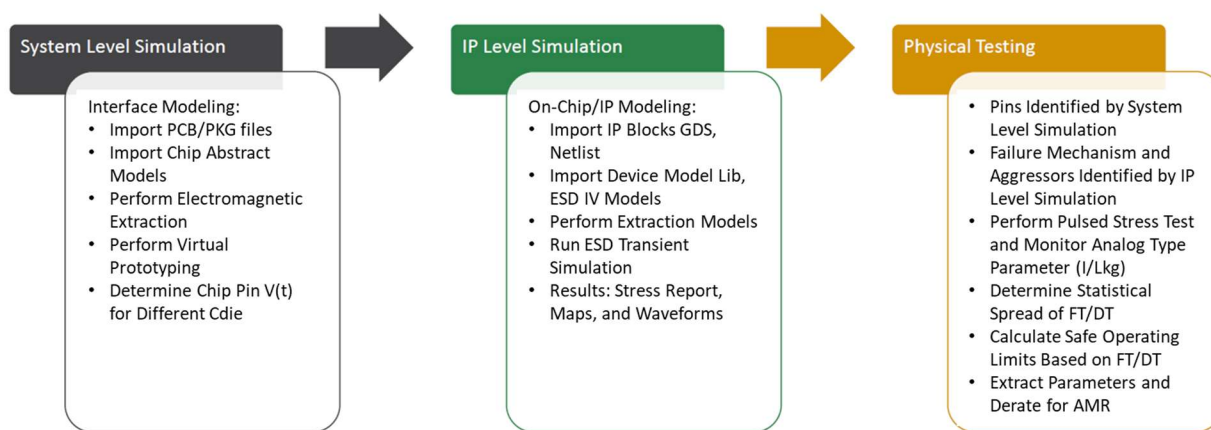


Figure A5: Simulation-Based Example Flow to Identify and Test at-Risk Pins

A system-level simulation can first be used, with the abstract chip model coupled to the extracted PCB/PKG models. The transient pin voltages can be captured by a system-level simulation. This can help the designer identify pins of interest for further detailed analysis and simulation. With this information available, the intellectual property (IP)-level simulation can be done in more detail. The IP-level simulation can use the transistor-level circuit for the IP block, and the transient waveforms captured at the pins from the system-level simulation can be applied to the IP block's pins for transient simulation. This can provide detailed information on transient voltages and currents in the transistors, which can be valuable for root cause analysis. More detailed simulation-based analysis at the device level can be performed by capturing the boundary conditions of the device and applying them to device-level TCAD simulations, for example, to understand the

voltage gradient across the device geometry. Finally, the physical testing of the chip/component can be done for the pin of interest, rather than testing all pins exhaustively, or perhaps test the pins of interest with a larger number of scenarios and input waveforms. In root cause analysis, the steps can be reversed. When a failure is observed in physical testing for a given set of pins with an input transient, system- and circuit-level simulations can be performed for the same set of pins with the specific input transient.

A.5 Validation Examples

A.5.1 Filament on a Junction

Figure A6 shows an ESD-robust protection diode structure subjected to multiple non-catastrophic strikes [Laasch 2009]. In this report, the event heating creates a non-uniform molten filament at the device junction, which does not significantly change the device's performance or leakage until enough pulses grow the damage filament beyond the PN-junction interface, at which point the device “shorts” out. The device was stressed with 80% of the maximum stress level. Initially, it showed no increase in leakage with a small number of stresses (see Figure A7). Even after the 199th stress, there was no change in leakage; only after the 200th stress did the leakage increase by 5 orders of magnitude.

It is a cumulative failure. The damage in the structure can be observed using failure analysis techniques, even though it cannot be measured electrically at the device's terminals.

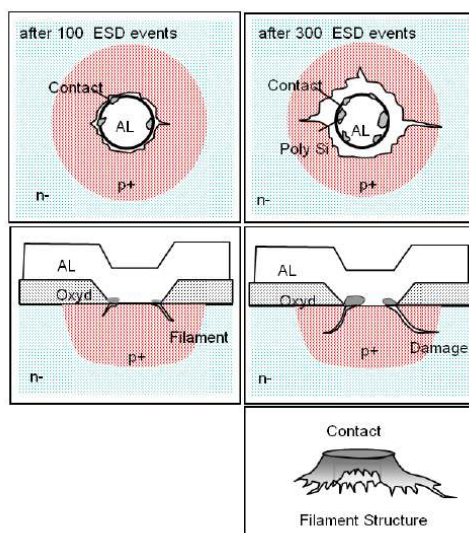


Figure A6: Damage Due to Filament Growth in a Bipolar Junction. (Laasch, et al., 2009)

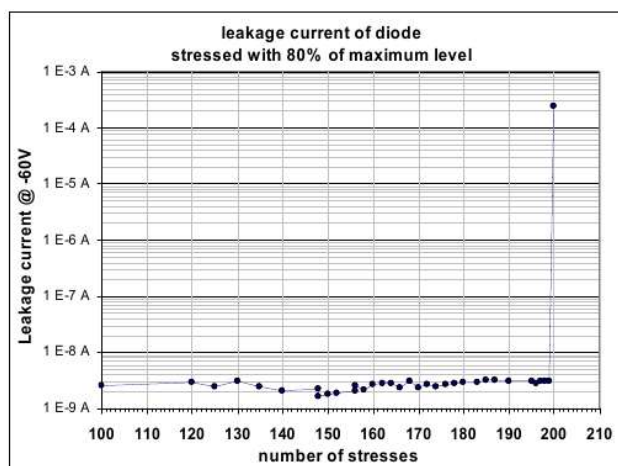


Figure A7: Cumulative Damage Building to Threshold Without Being Detected Via Leakage

A.5.2 Thin Copper Metal Interconnect

As technology scales toward increasingly compact and efficient ICs, the backend of the line is posing severe constraints, with the backend now playing a major role in ESD network behavior. For this reason, the definition of suitable design rules for metal interconnections is well known to be a fundamental item to be addressed: self-heating analysis and the interaction between ESD stresses and electromigration performance should be considered over a wide range of stress durations, including outside the typical ESD regime. Applying a TLP pulse allows characterization of isolated metal strips, providing information such as current and power capability as a function of applied stress duration, and the metal's self-heating as a function of injected current and stress time. An example of this analysis on a thin copper metal interconnection is shown in Figure A8. Starting from a TLP characterization at different pulse durations, it is possible to extract its power capability as a function of the applied stress time.

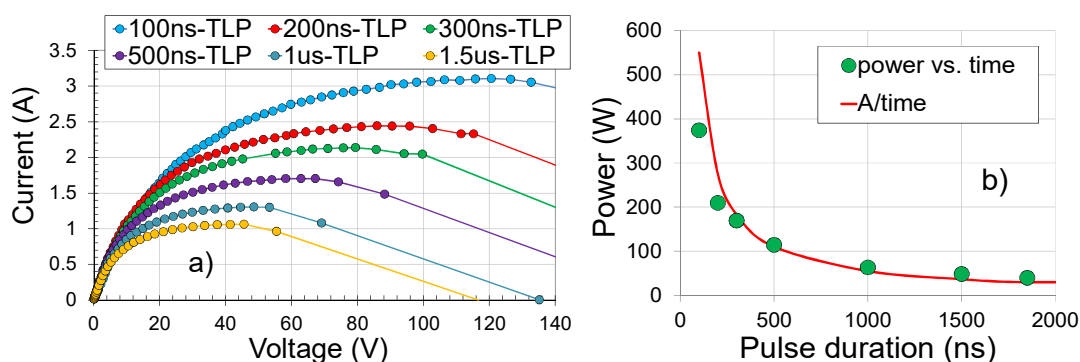


Figure A8: Thin Copper Metal Strip: a) I-V Curves vs. Time; b) Power vs. Time

The metal degradation mechanism can also be investigated in detail [Di Biccari2015]: no degradation is visible on the copper strip, even close to the maximum current point (MCP), where the melting temperature is reached inside the metal. Exceeding this limit, voids start to appear at

copper grain boundaries, and their size and number increase with temperature (see Figure A9). Finally, copper migration occurs, and the strip is destroyed at the “metal open” point.

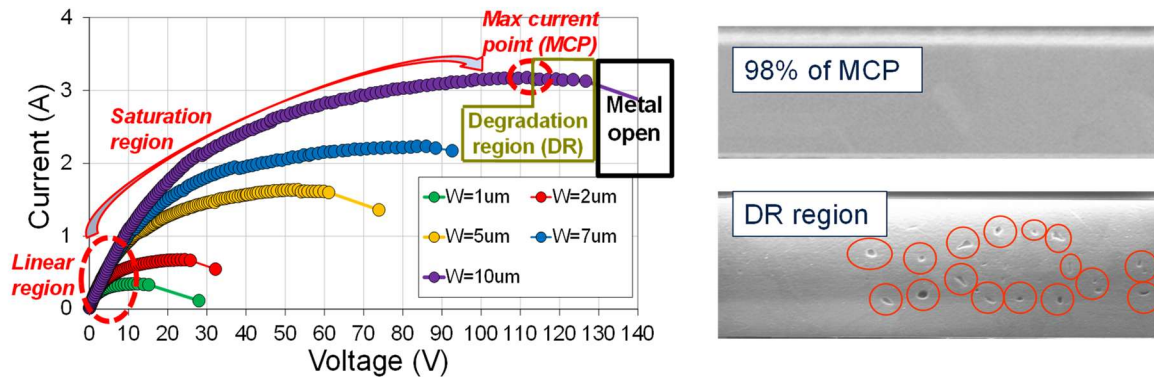


Figure A9: Thin Copper Metal – Degradation Mechanism

When stress pulses in the ESD regime are applied, the actual position of metal destruction is inconsistent with a simple metal-melting mechanism. By combining 3D TCAD simulations, characterization data, and physical analyses, the physical mechanism underlying the final metal opening can be thoroughly investigated: a thermomigration effect occurs at the points of maximum temperature gradient within the copper metal strip (see Figures A10 and A11).

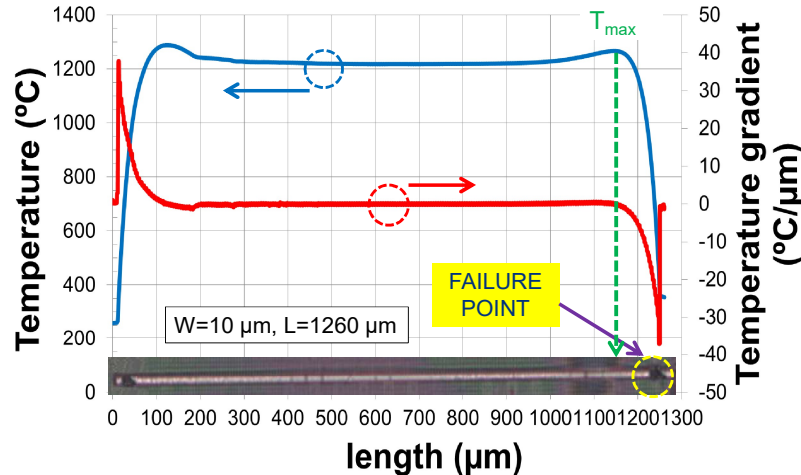


Figure A10: TCAD vs. Experimental Data – Failure Mechanism in Thin Copper Metals [Di Biccari2015]

A.5.3 Audio Pre-Amplifier Latch-up Weakness

The customer complained about several 0-km failures in a 4-channel audio preamplifier; the devices were not functioning. Electrical analysis indicated problems with the supply line, and failure analysis showed multiple damage points on a line derived from the main supply, Vbat.

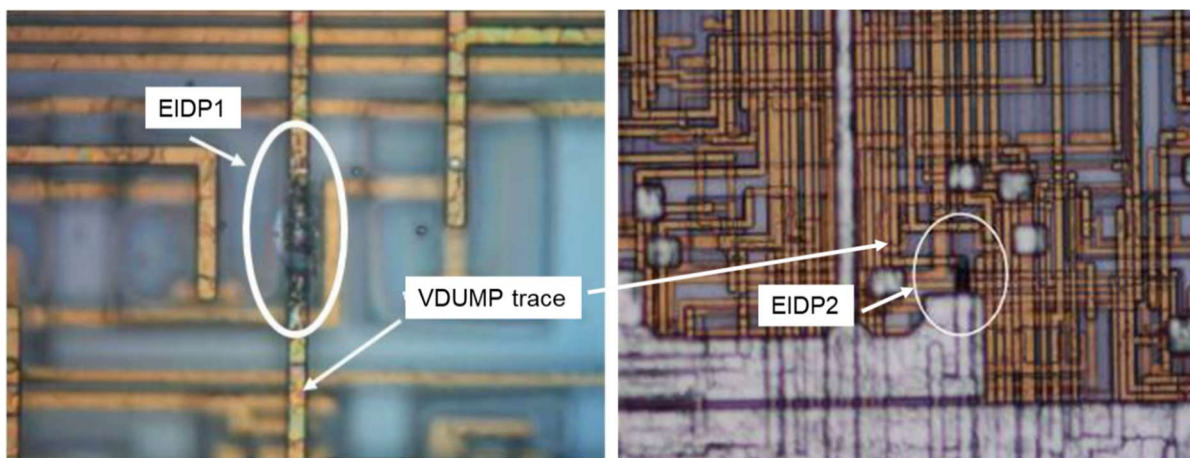


Figure A11: Field Failure Returns

The product AMR was 28 volts, the same as other similar devices on the market, and device and system reliability trials showed no anomalies. Therefore, several trials on supply lines were performed above qualification limits to verify any weaknesses in board design or handling processes. Physical signatures from these additional trials were not compatible with field returns, either because they were too energetic, completely burning the line, or because they involved ESD protection. A deeper analysis of the signatures showed that line burns were caused by local latch-up due to poor layout.

To activate this phenomenon, custom equipment was used. The equipment can send square pulses of a specified duration, superimposed on the nominal voltage, while the device is running on the HTOL board (see Figure A12). Pulse characteristics are depicted in Figure A13.

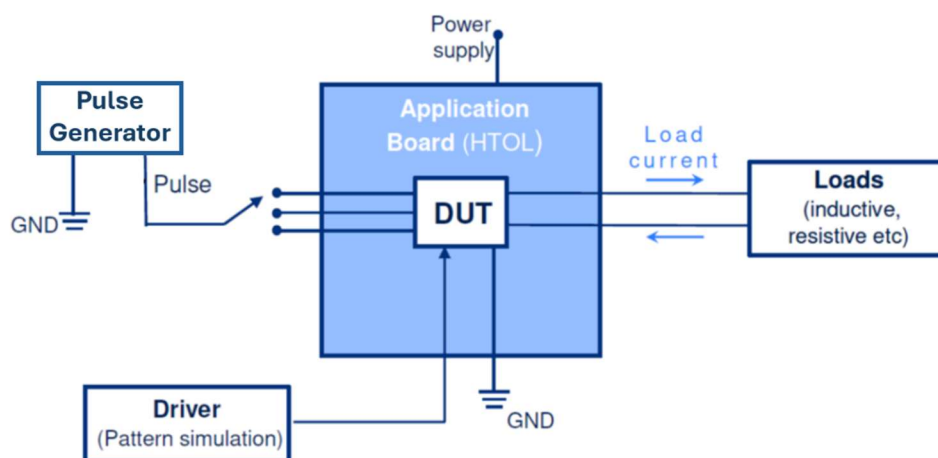


Figure A12: Equipment Schematic

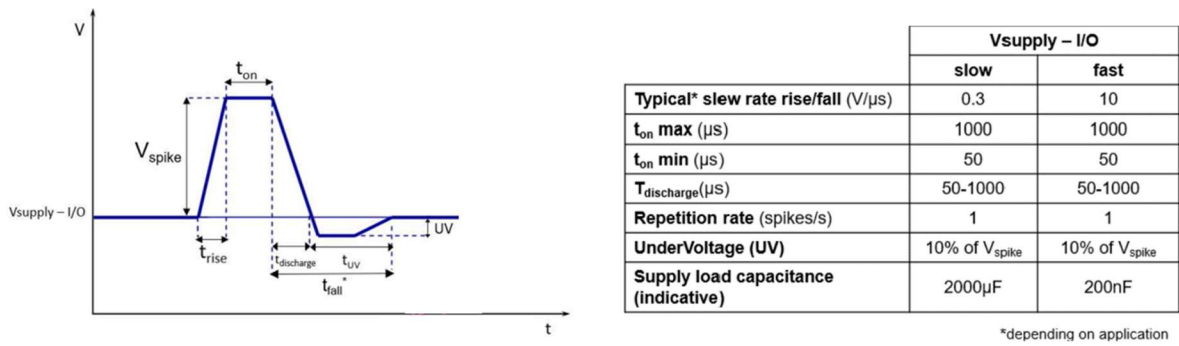


Figure A13: Pulse Characteristics

These trials led to very good reproduction of field failures by applying stresses ranging from 26.3 volts to 33.2 volts, with durations from 50 to 400 μs.

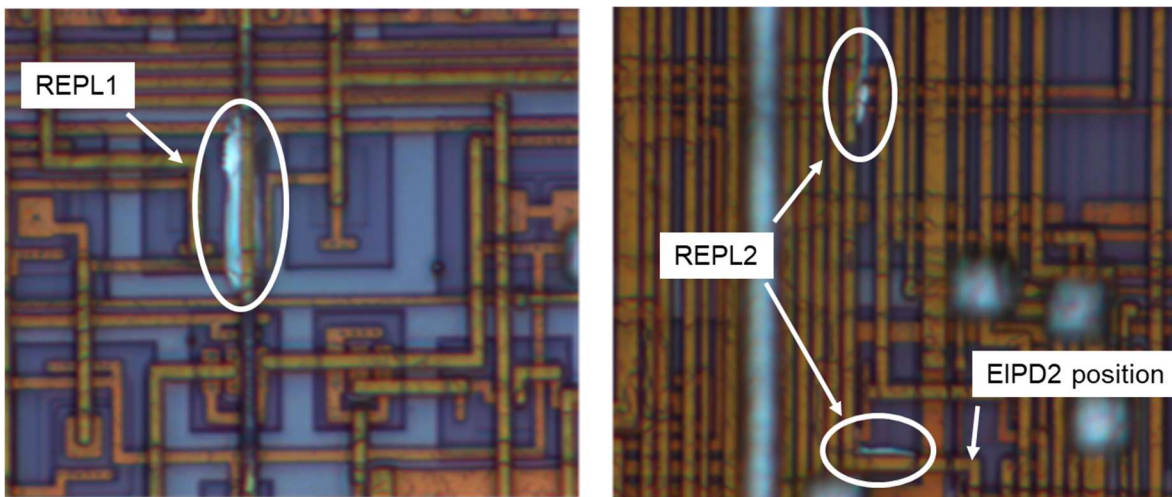


Figure A14: Field Failure Replications (left: 28.9 V and 400 us – right 26.3-33.2 V and 50-400 us)

Appendix B: Transient Stress Tests at Device and System Level

Andrea Boroni, STMicroelectronics

B.1 Transient Stress Test at Device Level

B.1.1 Human Body Model (HBM) [JS001]

HBM is meant to simulate charged personnel handling a device and discharging through it. Several standards are available, but all require applying stress in the same way. Charged capacitance is discharged using a relay through the device; the stress is applied to one pin while one (or more) other(s) is grounded (see Figure B1 (a)). The result for a short (see Figure B1(b)) is a double exponential with a rise time of 2-10 ns and a decay time constant of 150 ns. The ringing in the waveform is due to parasitic inductance in the system used to capture this realistic waveform. Peak current depends on the capacitor's initial charge with a ratio of 0.67 A/kV.

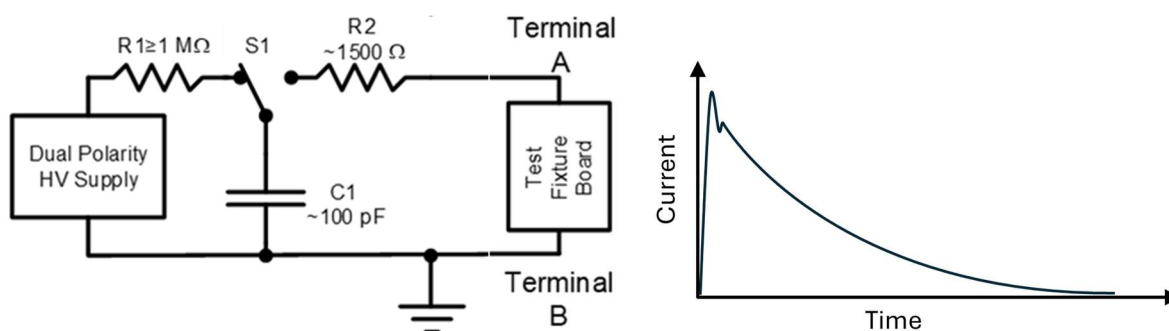


Figure B1: (a) HBM Schematic and (b) Typical Waveform on a Short

B.1.2 Charged Device Model (CDM) [JS002]

A major threat in the industry nowadays is the automated handling of devices, which can contact a metallic surface at a different potential, causing ESD stress. The discharge shape varies depending on a variety of factors, including but not limited to product size, relative position, and humidity. CDM stress, as defined in the current standard, has been shown to represent the worst-case scenario for such stress. Since the discharge waveform depends on capacitance, equipment performance is verified using standard 7.2 pF and 55 pF disk capacitors. The expected waveform and related parameters are depicted in Figure B2, and specifications are summarized in Table B1.

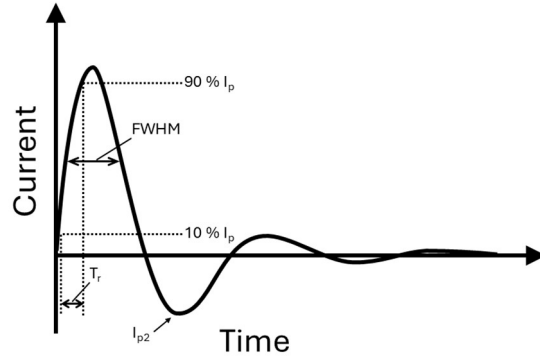


Figure B2: CDM Characteristic Waveform and Parameters

Table B1: CDM Waveform Characteristics for a High Bandwidth (≥ 6 GHz) Oscilloscope

Test Condition		TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	I_p	1.4-2.3	2.3-3.8	2.9-4.3	4.8-7.3	6.1-8.3	10.3-13.9	9.2-12.4	15.5-20.9	12.2-16.5	20.6-27.9
Rise time (ps)	T_r	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350	< 250	< 350
Full width at half maximum (ps)	FWHM	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900	250-600	450-900
Undershoot (A, max. 2nd peak)	I_{p2}	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p

B.2 Transient Stress Tests at the System Level

In this section, only the IEC and ISO stress tests will be discussed.

B.2.1 IEC System Level Stress

B.2.1.1 IEC 61000-4-2 [IEC6100042] Electrostatic Discharge Immunity Test

ESD is the sudden transfer of electrostatic charge between bodies at different potentials. ESD has the characteristics of high current flow for a short period. The primary purpose of the IEC 61000-4-2 test is to determine a system's immunity to external ESD events during operation. IEC 61000-4-2 specifies testing using two coupling methods:

- contact discharge
- air gap discharge.

IEC 61000-4-2 defines an ESD generator, often called an ESD gun, for use in system testing. Testing is performed by charging the generator's internal capacitor and discharging it through an internal resistor into the strike tip. Contact discharge is performed by touching the discharge tip directly to conducting parts of the system under test and triggering the strike. Conversely, air discharge is performed by triggering the gun and then moving the discharge tip towards non-conducting surfaces under test until arcing occurs. IEC 61000-4-2 only specifies direct stressing of system input and output pins under limited conditions, but system manufacturers often do direct

pin stressing. The air-discharge method better represents an actual ESD event than the contact-discharge method. However, it is not as repeatable due to several factors, including humidity, temperature, barometric pressure, distance, and the rate of approach to the unit. Gap distance, surface conditions, and humidity influence the statistical time lag. The statistical time lag, in conjunction with the speed of approach, determines whether actual sparking occurs at distances below the static breakdown voltage.

The specifications of the generator, as well as the environment and testing area, are well-defined. The generator (see Figure B3 (a)) shall comply with the following specifications:

- energy storage capacitance (C_s): $150 \text{ pF} \pm 10\%$;
- discharge resistance (R_d): $330 \Omega \pm 10\%$;
- charging resistance (R_c): between $50 \text{ M}\Omega$ and $100 \text{ M}\Omega$;

and the waveform on a specific target shall look like Figure B3 (b).

The test shall be carried out using the setup depicted in Figure B4 (a) for table-top systems and Figure B4 (b) for floor-standing equipment.

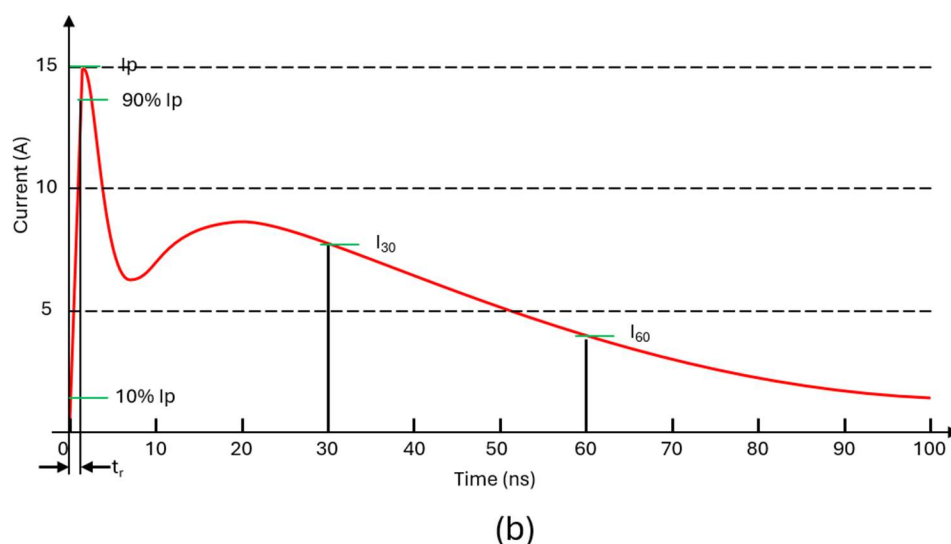
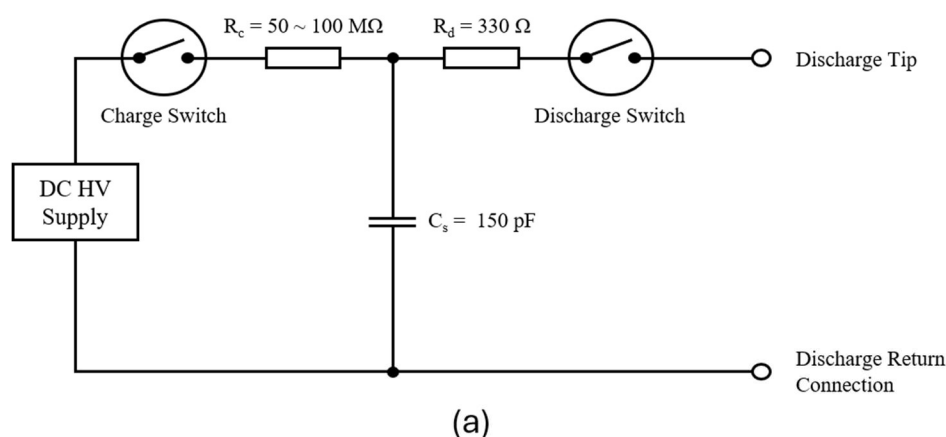


Figure B3: (a) IEC 61000-4-2 Generator (b) IEC 61000-4-2 Typical Waveform

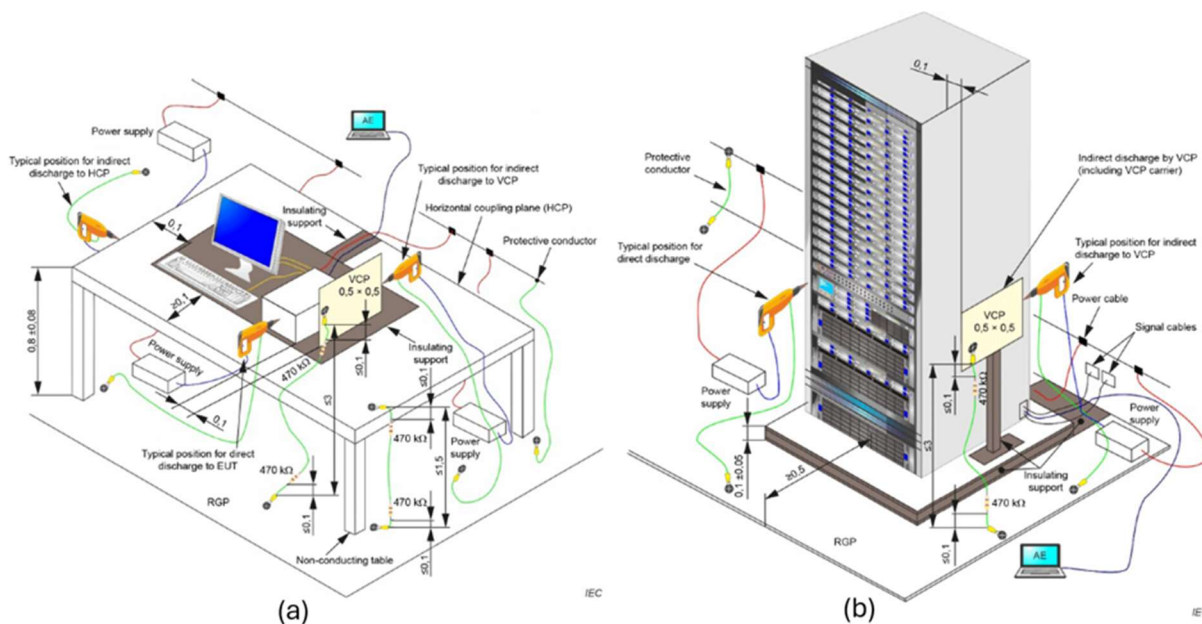


Figure B4: (a) Setup for Table-Top Equipment (b) Setup for Floor-Standing Equipment

Electrostatic discharges are applied to the equipment under test (EUT) at points and surfaces that are normally accessible to the operator under normal operating conditions. These discharges are also applied to the metal horizontal and vertical coupling planes (HCP, VCP). The voltage levels are gradually increased until the selected maximum severity level is reached. Discharges to the EUT and coupling plane are performed at a minimum of 1-second intervals at each polarity.

B.2.1.2 IEC 61000-4-4 [IEC6100044] Electrical Fast Transient/Burst Immunity Test
Industrial, office, and even household applications widely use cables in power delivery and data communications. Electrical fast transient (EFT) events from the environment or from surrounding power or data cables may interrupt data communications through inductive or capacitive coupling.

EFT testing involves coupling a number of extremely fast transient impulses onto the signal lines to represent transient disturbances associated with external switching circuits that are capacitively coupled onto the signal lines. This testing reflects switch contact bounce or transients caused by switching inductive or capacitive loads, both of which are common in industrial environments. The EFT test defined in IEC 61000-4-4 attempts to simulate the interference resulting from these types of events on the following ports:

- Supply ports
- IO (signal, control) ports (if cable length > 3 m)
- Earth ports

The simplified circuit diagram of the generator is given in Figure B5. The circuit elements C_c , R_s , R_m , and C_d are selected so that the generator delivers a fast transient under open circuit conditions and with a $50\ \Omega$ resistive load. The effective output impedance of the generator shall be $50\ \Omega$.

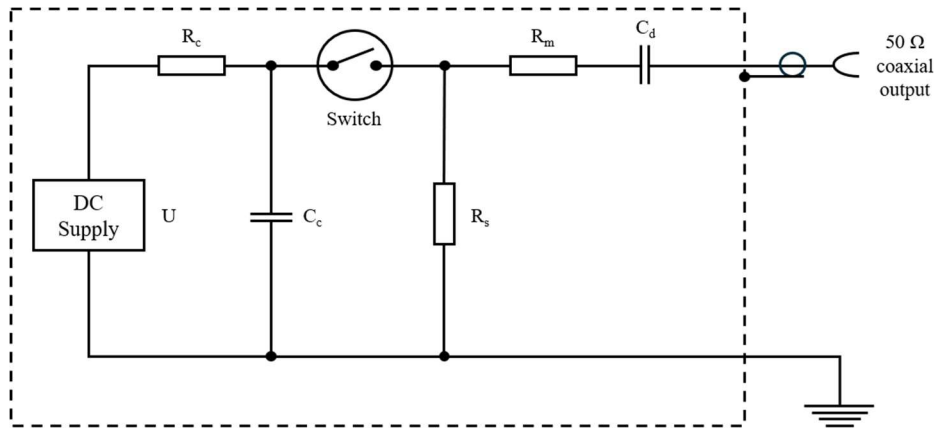


Figure B5: IEC 61000-4-4 Simplified Generator Circuit

The characteristics of the fast transient/burst generator shall be the following:

- Output voltage range with $1000\ \Omega$ load shall be at least 0.24 kilovolts to 3.8 kilovolts.
- Output voltage range with $50\ \Omega$ load shall be at least 0.125 kilovolts to 2 kilovolts.

The generator shall be capable of operating under short-circuit conditions without being damaged. Figure B6 (a) shows the EFT waveform. The output waveform consists of repetitive bursts of 5-kHz high-voltage transients. The bursts are spaced 300 ms apart, and each burst has a duration of 15 ms. Each pulse into a $50\ \Omega$ load is depicted in Figure B6 (b). The pulse has a rise time (t_r) of 5 ns and a pulse duration (t_w) of 50 ns, measured between the 50% points on the rising and falling edges of the waveform.

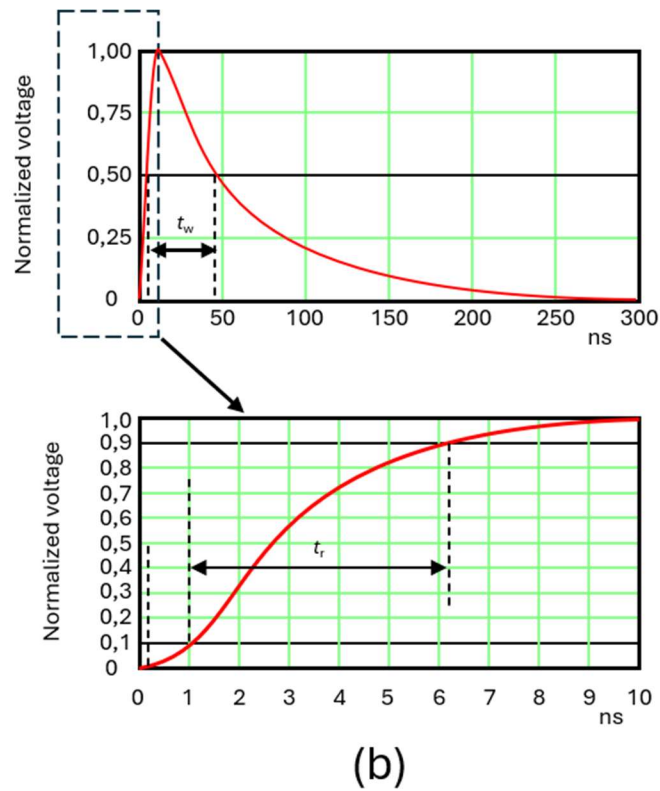
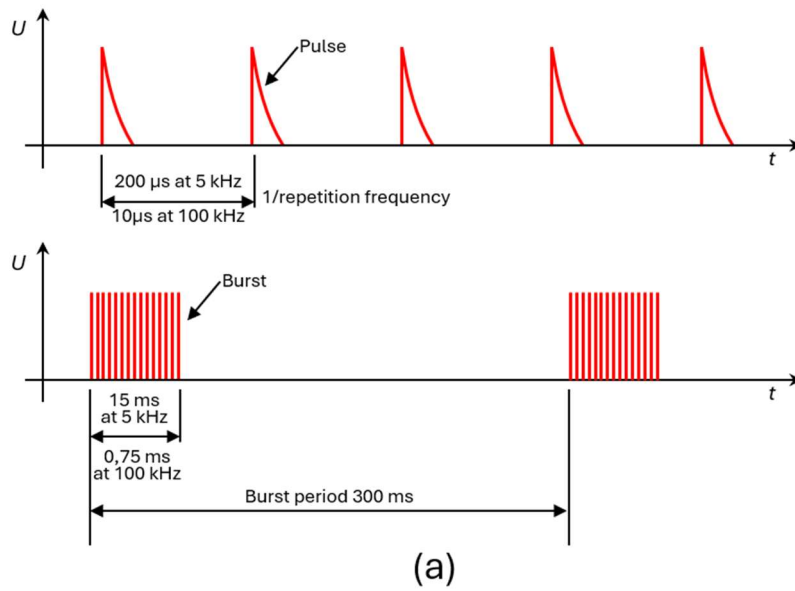


Figure B6: (a) Representation of an Electrical Fast Transient/Burst (b) Ideal Waveform Into a $50\ \Omega$ Load

The burst shall not be applied directly to the EUT, but shall be coupled to the input lines via a capacitive clamp. Also, the power supply shall be decoupled and filtered to avoid external noise that could cause unwanted interference. Figure B7 and Figure B8 show, respectively, coupling/decoupling networks for supplies and IO testing.

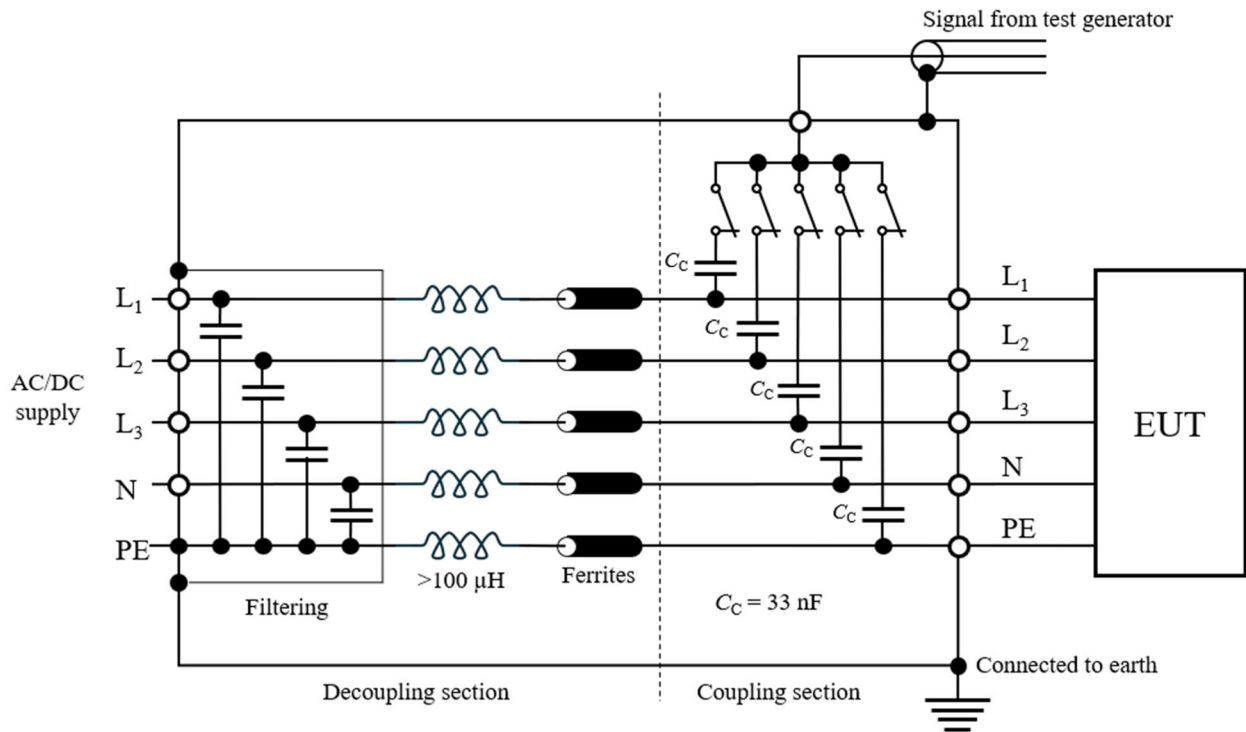


Figure B7: Coupling/Decoupling Network for AC/DC Power Mains Supply Ports/Terminals

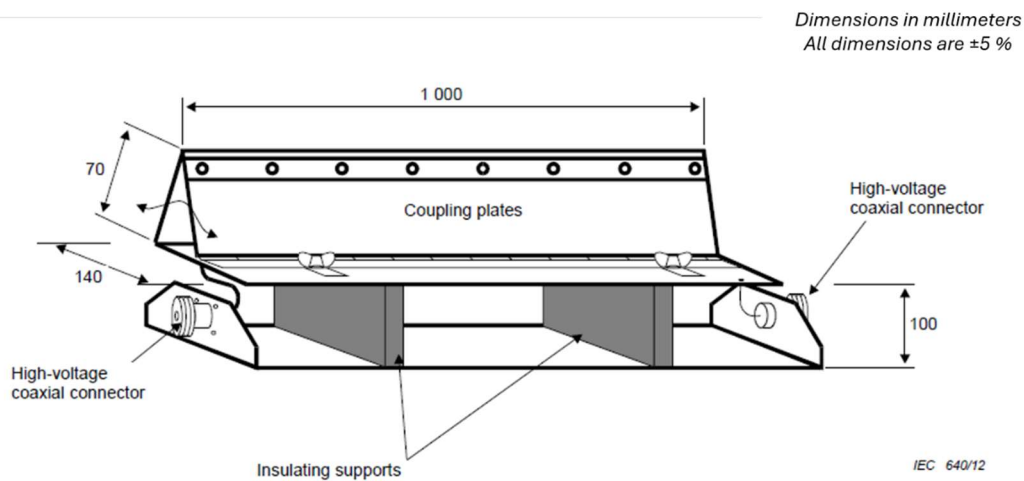


Figure B8: Capacitive Coupling Clamp for IO Testing

Unless otherwise mentioned, the floor-standing EUTs and equipment designed to be mounted in other configurations shall be placed on a ground reference plane and shall be insulated from it by an insulating support with a thickness of 0.1 ± 0.05 m, including non-conductive rollers/castors. Table-top equipment and equipment normally mounted on ceilings or walls, as well as built-in equipment, shall be tested with the EUT located 0.1 ± 0.01 m above the ground reference plane. Testing of large table-top equipment or multiple systems can be performed on the floor,

maintaining the same distances as for the test setup of table-top equipment. An example of a laboratory test setup is shown in Figure B9.

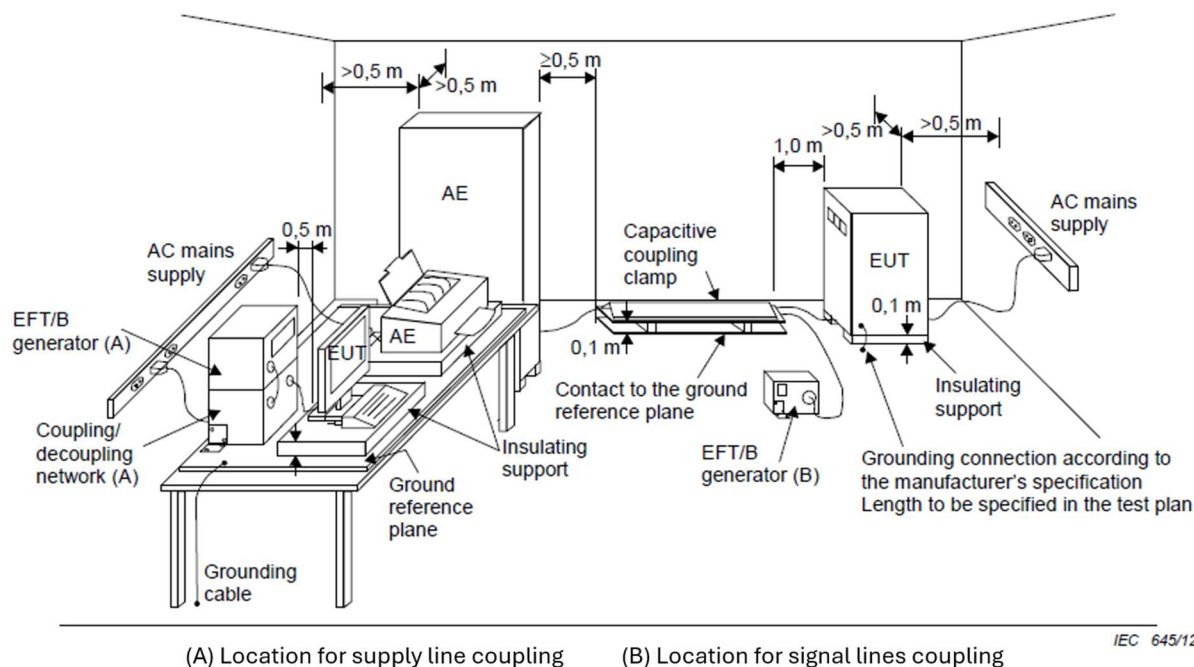


Figure B9: Example of a Test Setup for Laboratory-Type Tests

B.2.1.3 IEC 61000-4-5 [IEC6100045] Surge Immunity Test

Surge transients are caused by lightning strikes or the switching of major power systems. Lightning transients can result from high currents and voltages directly injected into the circuit by lightning strikes or indirectly injected from nearby sources, either through the electromagnetic field or via discharge to ground. Switching transients can result from power system switching, load changes in power distribution systems, or various system faults, such as short circuits and arcing faults in the installation's grounding system.

Two types of combination wave generators are specified. Each has its own particular applications, depending on the type of port to be tested. The 10/700 μ s combination wave generator is used to test ports intended for connection to outdoor symmetrical communication lines. The 1.2/50 μ s combination wave generator is used in all other cases. With the same peak power level, the 10/700 μ s surge contains more energy due to a longer pulse width.

Waveforms are specified as open-circuit voltage and short-circuit current and shall therefore be measured without the EUT connected. Notice that the surge pulse can have energy levels that are three to four orders of magnitude higher than the energy in an ESD or EFT pulse. Therefore, the surge transient is considered the most severe of the EMC transient specifications.

Also, the coupling/decoupling network (CDN) is another integral part of the test setup. The coupling network couples the surge pulse generated by the combination wave generator (CWG) to

the device under test (DUT), whereas the decoupling network sits between the CWG and the biasing equipment to prevent damage to the biasing equipment during the surge test.

1.2/50 μ s Combination Wave Generator (CWG)

A simplified CWG, depicted in Figure B10, has a power supply that charges the coupling capacitor, C_c , through a resistance. Upon closing of the switch, C_c discharges through a pulse-shaping network including R_{s1} , R_m , L_r , and R_{s2} . The values of these components are tuned to produce compliance waveforms under short-circuit and open-circuit conditions, as specified in IEC 61000-4-5.

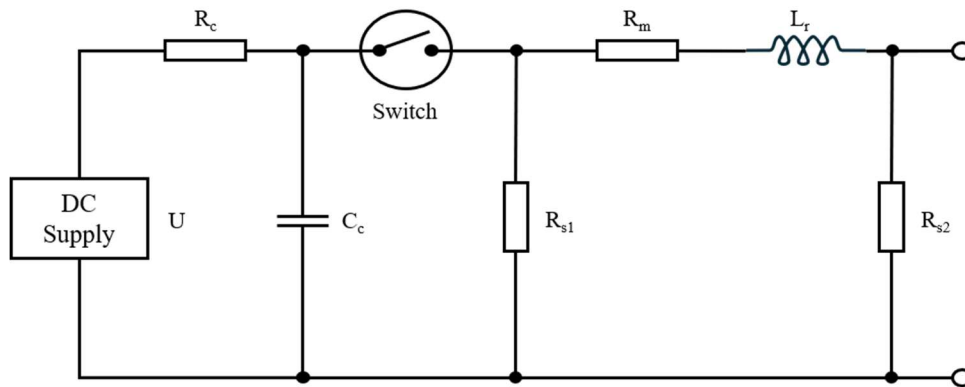
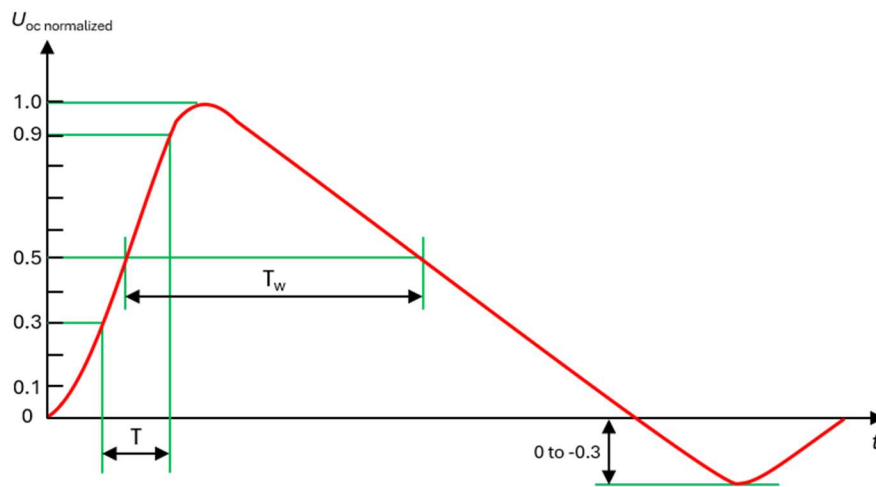


Figure B10: Simplified Circuit Diagram of the CWG (1.2/50 μ s)

This generator is intended to generate a surge having:

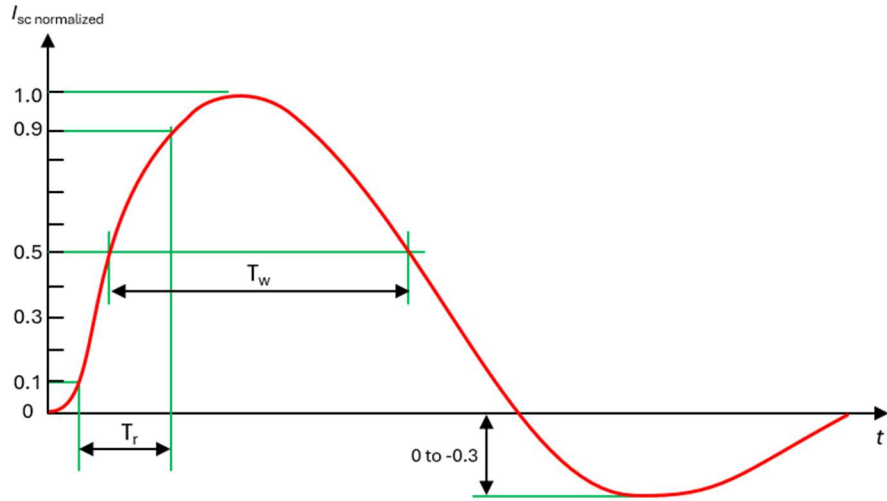
- an open-circuit voltage front time of 1.2 μ s and duration of 50 μ s (see Figure B11 (a))
- a short-circuit current front time of 8 μ s and duration of 20 μ s (see Figure B11 (b))



Front time: $T_f = 1.67 \times T = 1.2 \mu\text{s} \pm 30\%$
Duration: $T_d = T_w = 50 \mu\text{s} \pm 20\%$

NOTE: The value 1.67 is the reciprocal of the difference between the 0.9 and 0.3 thresholds.

(a)



Front time: $T_f = 1.25 \times T_r = 8 \mu s \pm 20 \%$
 Duration: $T_d = 1.18 \times T_w = 20 \mu s \pm 20 \%$

NOTE1: The value 1.25 is the reciprocal of the difference between the 0.9 and 0.1 thresholds.

NOTE2: The value 1.18 is derived from empirical data.

(b)

Figure B11: (a) Waveform of Open-Circuit Voltage and (b) of Short-Circuit Current at the Output of the (1.2/50 μ s) CWG

10/700 μ s Combination Wave Generator

The simplified circuit diagram of the generator is given in Figure B12. The values for the different components are selected so that the generator delivers the following surge.

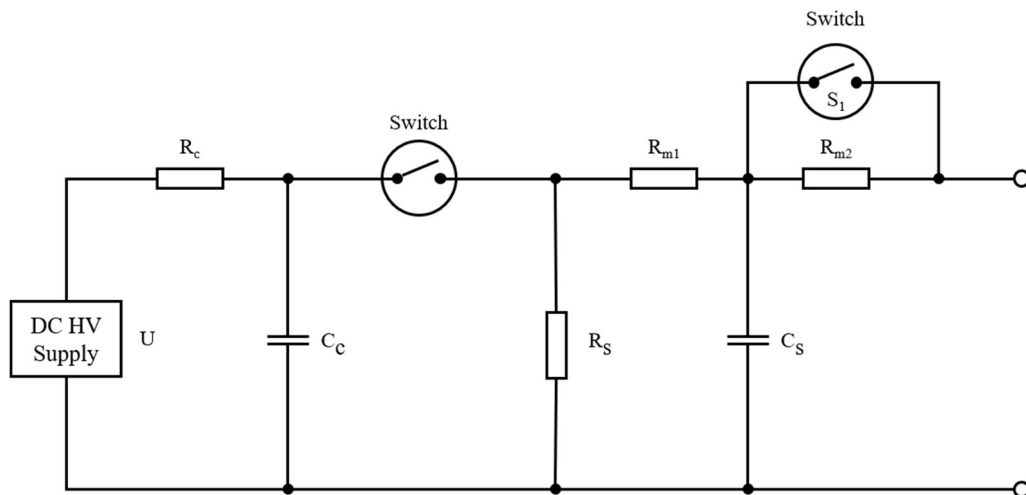


Figure B12: Simplified Circuit Diagram of the Combination Wave Generator (10/700 μ s)

This generator is intended to generate a surge with the following characteristics:

- an open-circuit voltage front time of 10 μ s and duration of 700 μ s (see Figure B13 (a))
- a short-circuit current front time of 5 μ s and duration of 320 μ s (see Figure B13 (b))

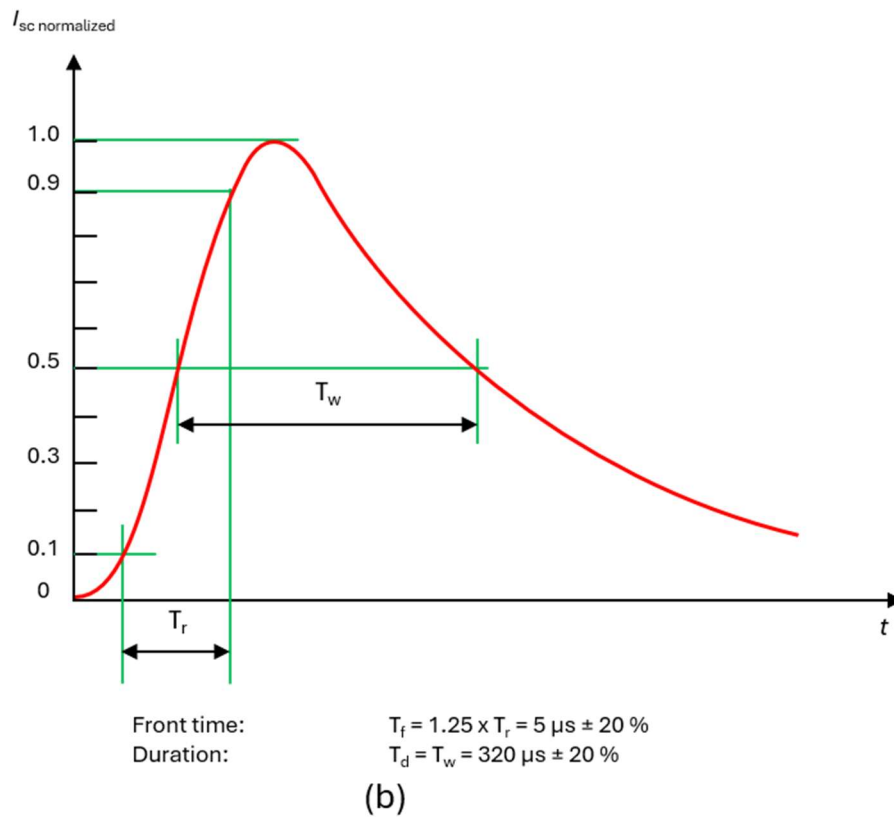
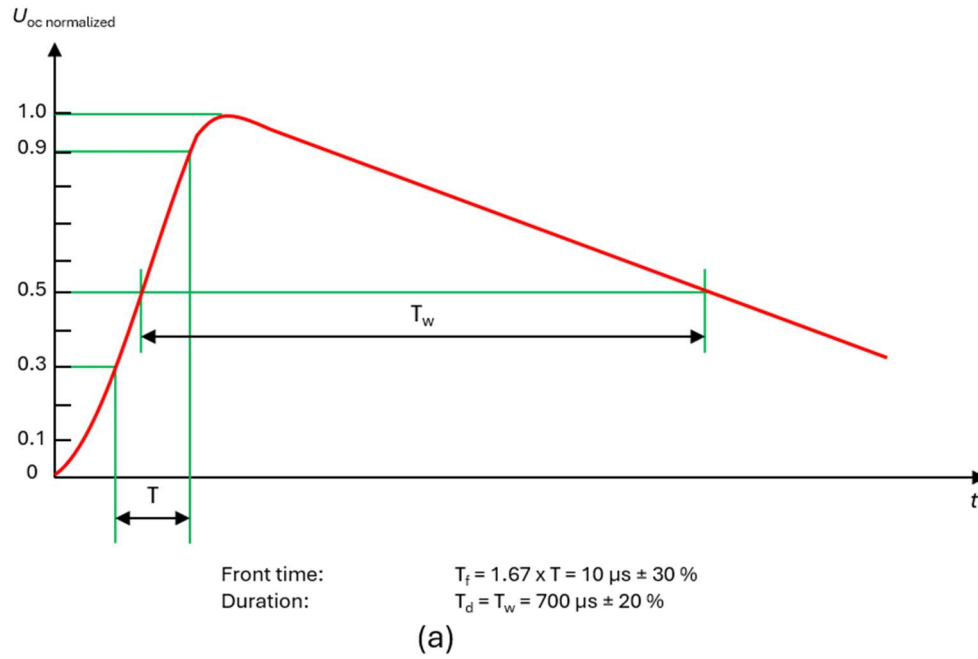


Figure B13: (a) Waveform of Open-Circuit Voltage and (b) of Short-Circuit Current at the Output of the (10/700 μs) CWG

B.2.2 ISO System Level Stress

B.2.2.1 ISO 10605 [ISO10605]

ISO 10605 is the international standard for testing the ESD immunity of electronic components in automotive applications. The standard, partly based on IEC 61000-4-2, simulates the discharge of a human body, both inside and outside a vehicle.

ESD applied to the DUT can directly influence the DUT. ESD applied to neighboring parts can couple into the DUT's supply and signal lines in the vehicle and/or directly into the DUT, so direct and indirect testing has been introduced in the standard.

The standard also requires testing both standalone modules and all the modules assembled in the vehicle.

The ISO 10605 generator is depicted in Figure B14. It is possible to use two different resistors to simulate different types of ESD events:

- A 2 k Ω resistor represents a human body discharging directly through the skin
- A 330 Ω resistor simulates a human body discharging through a metallic object.

The test is also done at two different capacitances:

- 150 pF capacitance represents a human body outside the vehicle
- 330 pF capacitance represents a human body inside the vehicle

The 330 pF and 330 Ω test has the highest energy or current of any of the ISO 10605 test parameters. The current waveforms on the calibration target are depicted in Figure B15, and the parameters are listed in Table B2.

Table B2: Contact Discharge Mode Current Specifications

Typical capacitance/ resistance values	Peak current/ charge voltage (A/kV)	Current at t ₁ / charge voltage (A/kV)	Current at t ₂ / charge voltage (A/kV)
150 pF / 330 Ω	3.75 $\pm$ 10%	2 (at t ₁ = 30 ns)	1 (at t ₂ = 60 ns)
330 pF / 330 Ω	3.75 $\pm$ 10%	2 (at t ₁ = 65 ns)	1 (at t ₂ = 130 ns)
150 pF / 2 k Ω	3.75 $\pm$ 30%	0.275 (at t ₁ = 180 ns)	0.15 (at t ₂ = 360 ns)
330 pF / 2 k Ω	3.75 $\pm$ 30%	0.275 (at t ₁ = 180 ns)	0.15 (at t ₂ = 800 ns)

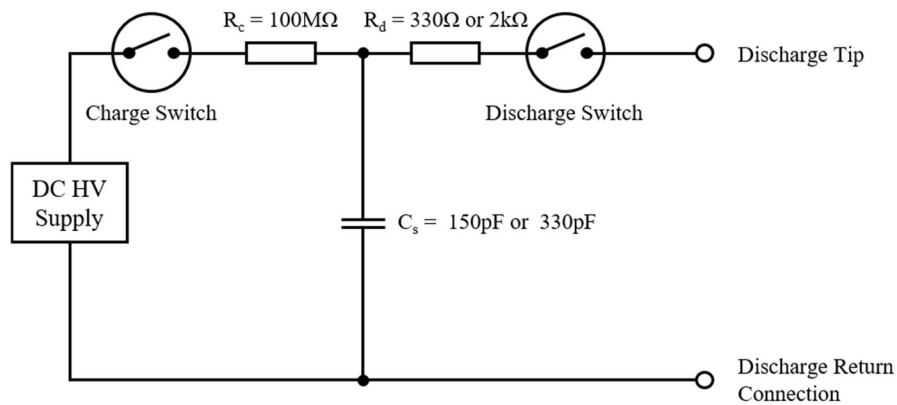


Figure B14: ISO 10605 Generator

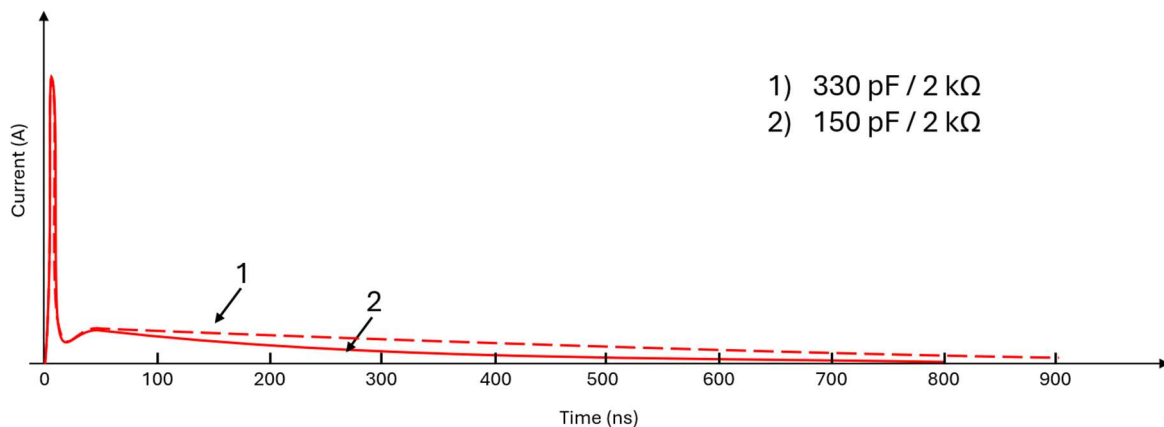
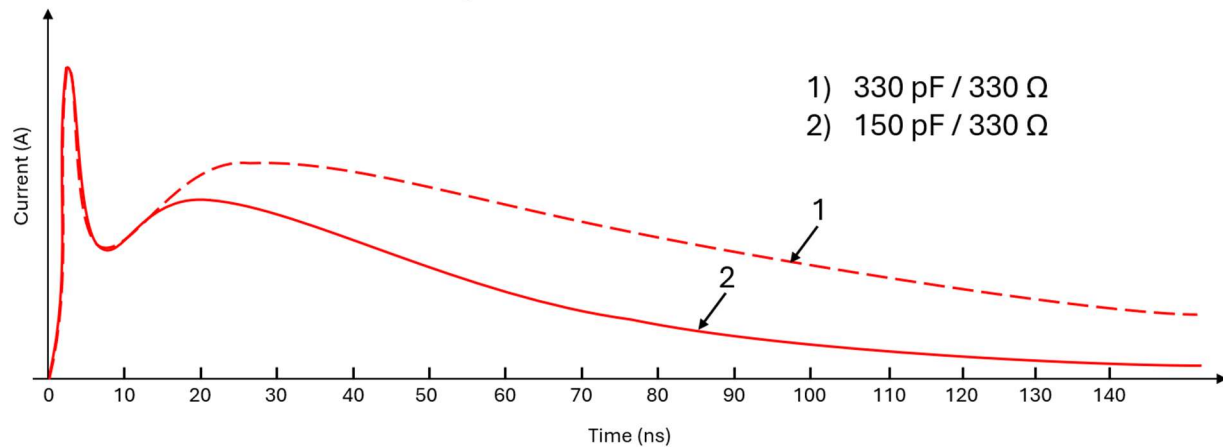


Figure B15: ISO 10605 Waveforms

Direct testing of both contact and air discharge shall be carried out on a bench, as depicted in Figure B16, while the system is running and connected to a battery. The RC network to be used depends on the position of the EUT in the vehicle. Discharges shall be applied to all specified test points with the equipment operating in normal modes.

Discharges to objects placed or installed near the DUT (indirect testing – Figure B16) are simulated by applying contact discharges of the ESD generator to a horizontal coupling plane (HCP). Contact

discharges shall be applied to the HCP at points on each side of the DUT. The ESD pulse should be applied to the edges of the HCP. The DUT shall be positioned on the HCP such that its closest surface is 0.1 m from the edge of the HCP receiving the discharge. The DUT may need to be repositioned during the test when applying ESD to the edge of the HCP, in order to maintain the 0.1 m spacing between the DUT edge and the edge of the HCP.

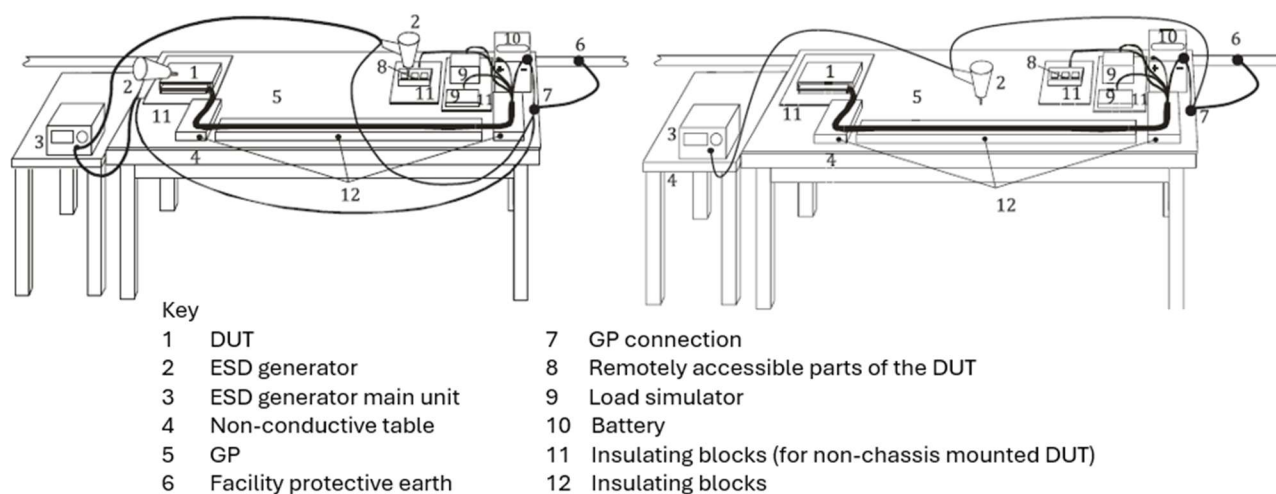


Figure B16: Test Setup Example for Testing Powered DUT Immunity to Direct (left) and Indirect ESD (right)

The standard also requires testing to simulate human discharges during assembly or service. This test consists of applying discharges directly to an unpowered DUT. The test shall be performed by direct-contact discharge on all pins and contacts, and/or by air-discharge mode on all surfaces and points that can be touched during the assembly process or in service. The test setup is simplified compared to the powered test (see Figure B17).

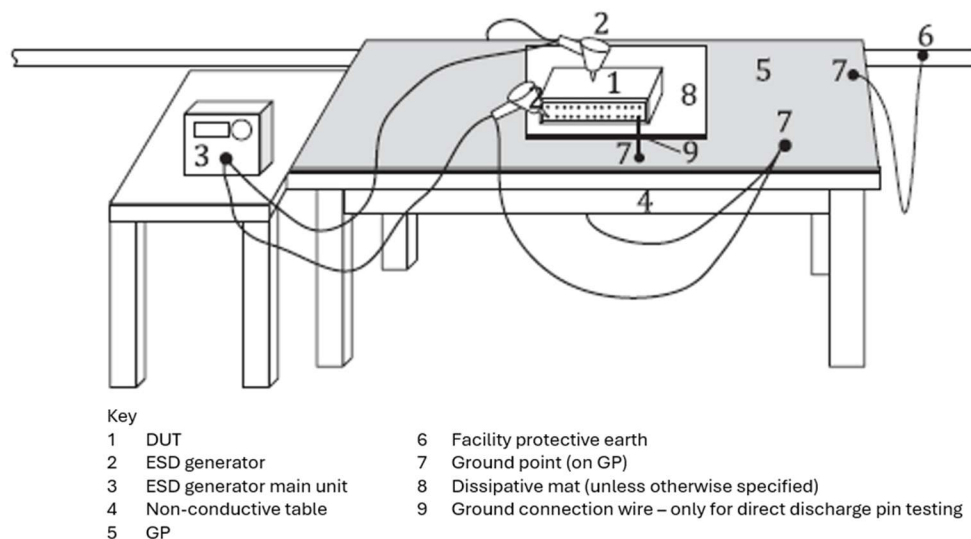


Figure B17: Test Set-up Example for Packaging and Handling Sensitivity Classification

Peak voltage varies depending on the DUT's classification. DUTs with more critical functions are subjected to larger amplitude voltages.

Pulse 2a

Pulse 2a (see Figure B19) simulates transients caused by sudden interruptions of current in an inductive component connected in series with the DUT. The positive Pulse 2a is superimposed on the vehicle DC supply voltage. This pulse usually occurs in the vehicle when the ignition is switched on.

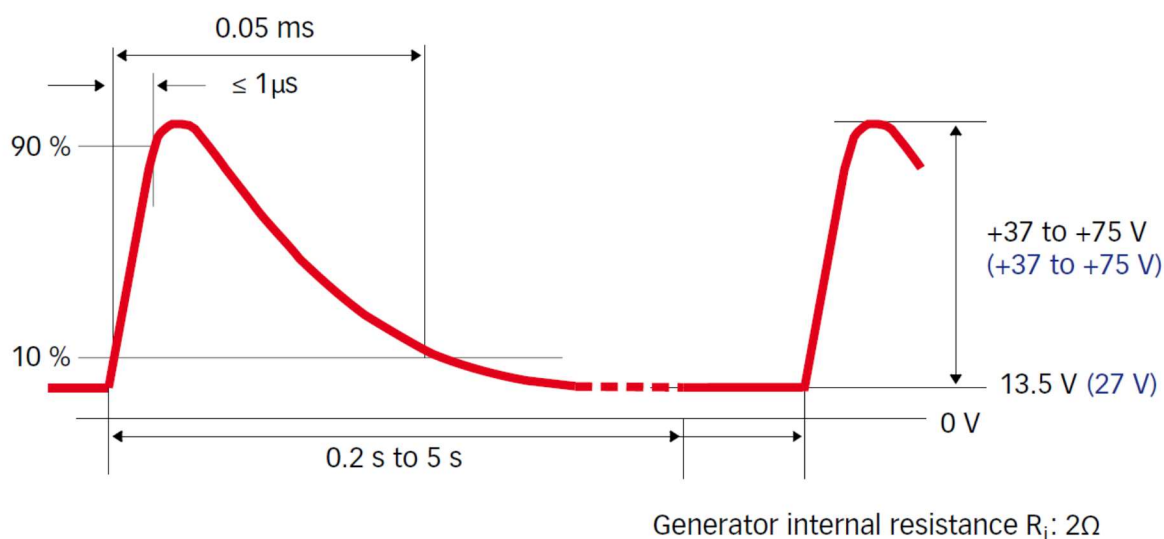


Figure B19: Pulse 2a

Pulse 2b

Pulse 2b (see Figure B20) is frequently called the "PM motor rundown pulse" or the "motor shutdown pulse". This name refers to a permanent-magnet motor, such as the cooling or heating system blower motor, that acts as a generator once power to the motor is removed. It was first noticed in automotive radios as a "burring" noise through the radio speaker when the ignition key is first turned off with the blower fan operating. It is a result of the direct coupling of the radio speaker to the audio output transistors, rather than using a coupling transformer. This type of audio output design was first utilized in the early 1970s. The blower motor continues to supply DC power to the audio system even though the DC supply has been removed. As a result, the auto engineers required testing the radio and suppressing the phenomenon. Subsequent specifications added testing of the motor shutdown pulse for all electronic modules, and as a result, it has become a requirement in international test specifications as well.

The time needed to drop from 90% to 10% of the nominal voltage (either 12 volt or 24 volt) shall be (t_f) 1 ms $\pm$ 0.5 ms, so the slope of the voltage just after DC supply removal is higher than the following rise.

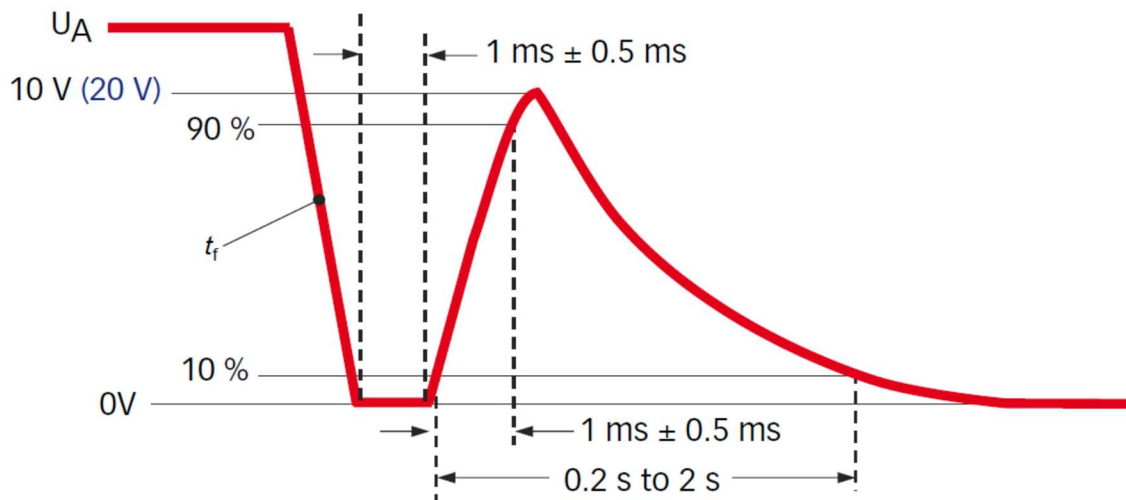


Figure B20: Pulse 2b

Pulse 3a and 3b

Pulse 3a and 3b (see Figure B21) are negative and positive pulses that are identical in characteristics except for their polarity. They are similar to pulses identified in industrial and commercial EMC testing specifications as high-frequency switching transients that occur on AC power mains and are called electrical fast transients (EFT). In the vehicle, their origins are similar in that these fast transients occur as arcing across contact points in mechanical switches and relays. Distributed capacitance and inductance in the wiring harness influence these transients since the transients have rise and fall times (< 5 ns) in the radio frequency range (> 200 MHz). As a result, these transients are coupled by conduction and via radiation within the DUT. This can cause timing errors, memory losses, and other functional errors within the DUT.

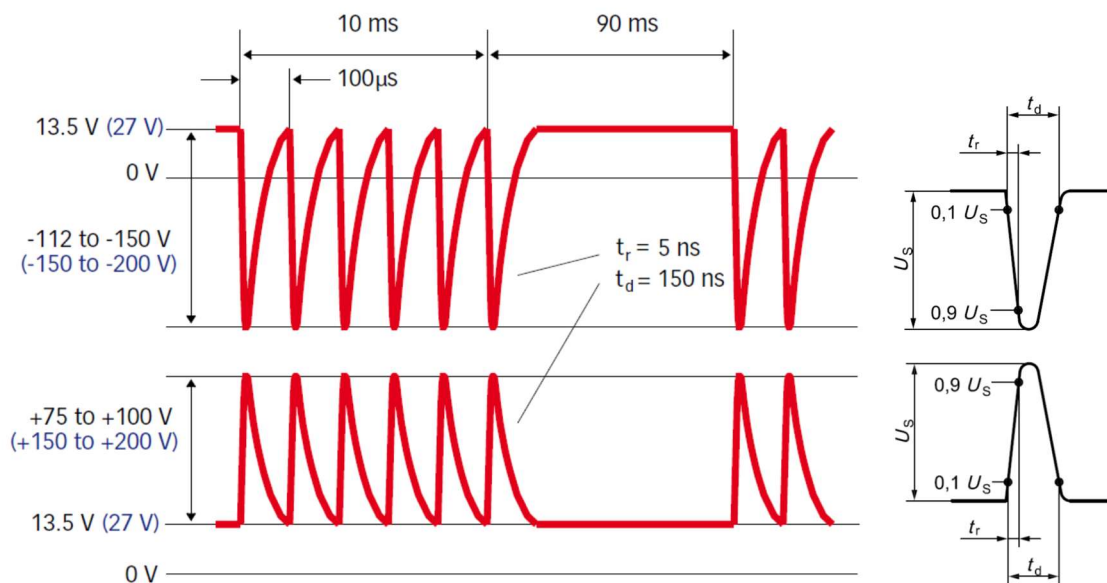


Figure B21: Pulse 3a (top) and 3b (bottom)

B.2.2.3 ISO 16750-2 [ISO16750]

This part of ISO 16750 describes the potential environmental stresses and specifies tests and requirements recommended for the specific mounting location on/in the road vehicle. This part of ISO 16750 describes the electrical loads. ISO 16750 contains several pulses; however, in this section, only those with a fast transient will be analyzed.

Superimposed Alternating Voltage

ISO 16750-2 Superimposed AC test simulates residual large AC ripple current on a DC supply, such as from switching supplies or traction motor drives.

An AC sine wave is superimposed on the battery voltage and swept logarithmically from 50 Hz to 25 kHz and back over a period of 120 seconds (60 seconds up, 60 seconds down), then repeated 5 times (see Figure B22).

The test defines four severity levels:

- severity 1: peak to peak voltage, U_{PP} , of 1 volt, both for 12 volts and 24 volts
- severity 2: peak to peak voltage, U_{PP} , of 4 volts, both for 12 volts and 24 volts
- severity 3: peak to peak voltage, U_{PP} , of 10 volts, for 24 volts only
- severity 4: peak to peak voltage, U_{PP} , of 2 volts, for 12 volts

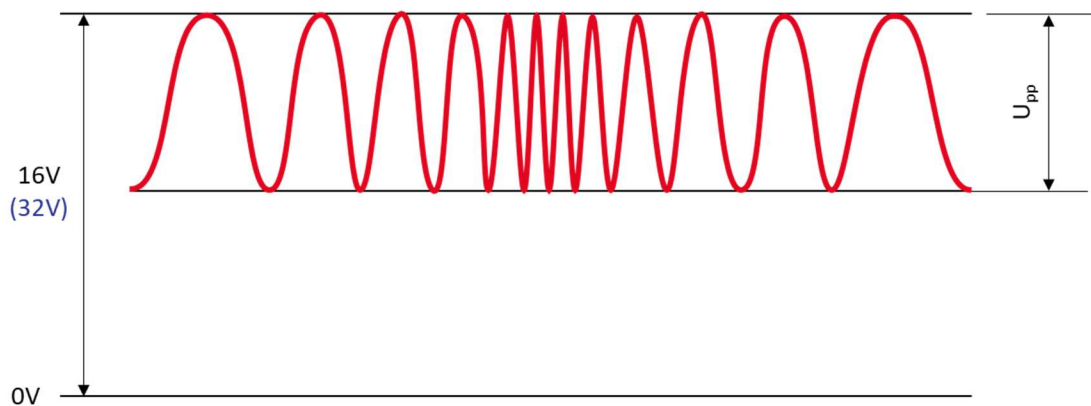


Figure B22: Test Voltage With Superimposed Sinusoidal AC Voltage

Starting Profile

When the starter motor of a vehicle with an internal combustion engine is engaged, there is a very large current draw from the vehicle battery (about 400 amps). Due to the large current draw and the vehicle's wiring resistance, the DC supply voltage to the vehicle's electronic systems is reduced. This happens especially in cold weather.

Frequently known as the "crank pulse" (see Figure B23), the reduction in voltage to the electronic modules can cause malfunctions if it is not properly accounted for. Also, different severity levels are defined based on the system's nominal voltage.

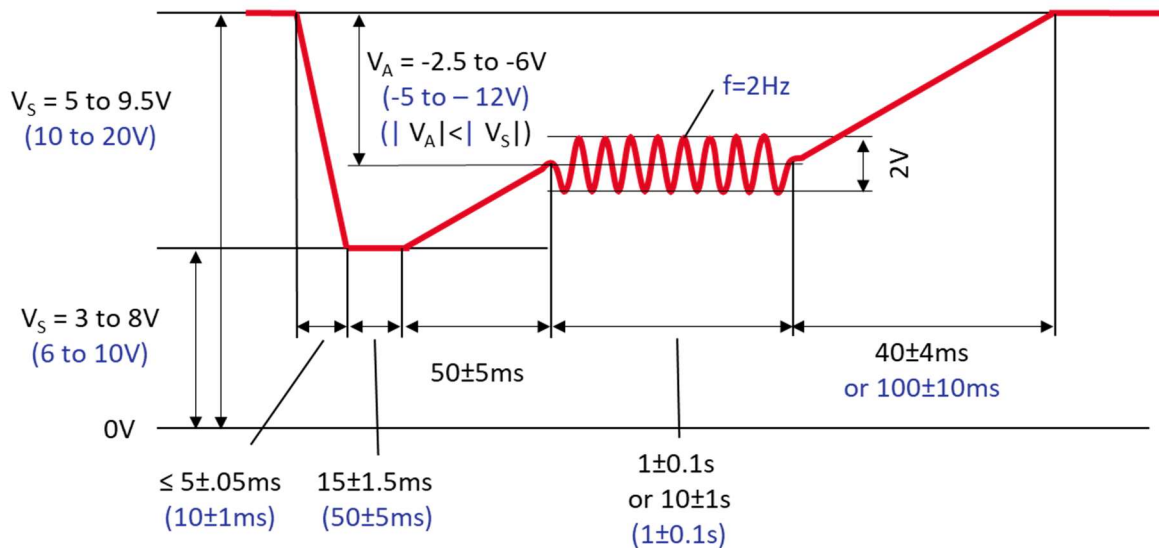


Figure B23: Starting Profile or “Crank Pulse”

Load Dump

When electronic systems first appeared in vehicles in the early 1960s, mysterious failures occurred periodically. The randomness and frequency of the failures led some auto manufacturer managers to doubt the cost-effectiveness of using electronic components in the largely mechanical auto environment. In one case, early versions of electronic ignition systems were withdrawn from the vehicle design because of excessive failures. Since solid-state devices were in the early stages of their use, this tack seemed prudent. At the same time, alternators replaced generators as the primary source of battery charging. Alternators provided charging currents that were more consistent with overall engine RPM ranges.

Failure analysis of the damaged electronic systems revealed that transistors directly connected to the DC supply lines were completely "blown" or destroyed by excessive energy. The energy required to blow the transistors was much higher than any known available energy in the vehicle's DC supply system. An investigation into the automotive charging system revealed that when the alternator is charging a fully or nearly discharged battery, a large amount of current flows into the battery. When the battery cables are corroded, frayed, or otherwise disconnected from the charging battery, a very high-energy pulse is impressed on the vehicle's DC system. This high-energy pulse is called "load dump". The load dump pulse has enough energy to destroy an unprotected electronic system. This is why early electronic systems failed. As a result, auto manufacturers later added suppression Zener diodes to the alternator output. The diodes clamped the load dump pulse to a maximum of about 32 volts, reducing its damaging effect. In an unsuppressed system, the load dump pulse can exceed 100 volts. Also, the auto manufacturers added a load dump pulse test requirement for the electronic modules.

The standard specifies both conditions:

- Test A: without centralized load dump suppression (see Figure B24 (a))
- Test B: with centralized load dump suppression (see Figure B24 (b))
(cutting voltage depends on the suppression network)

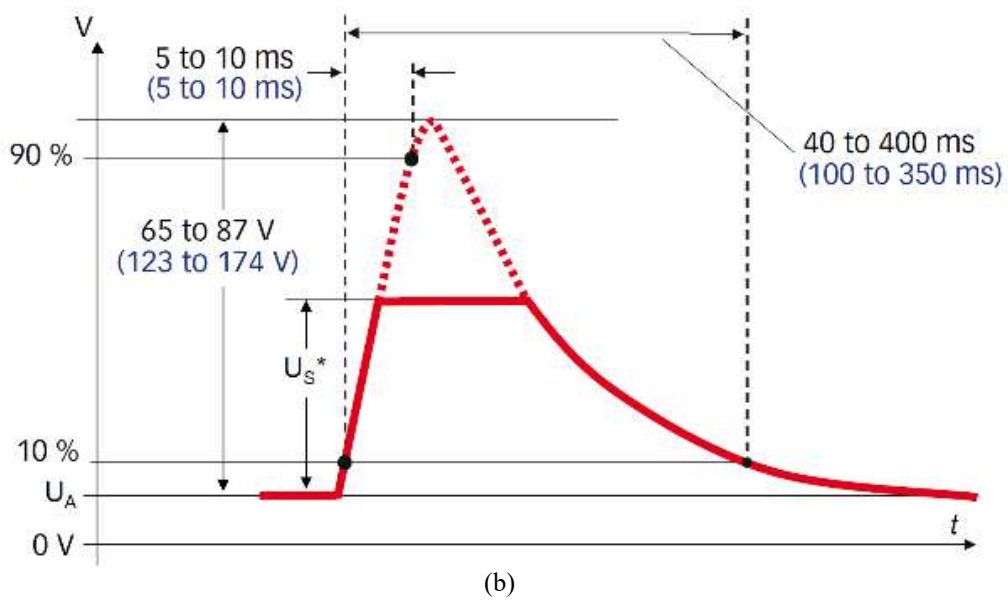
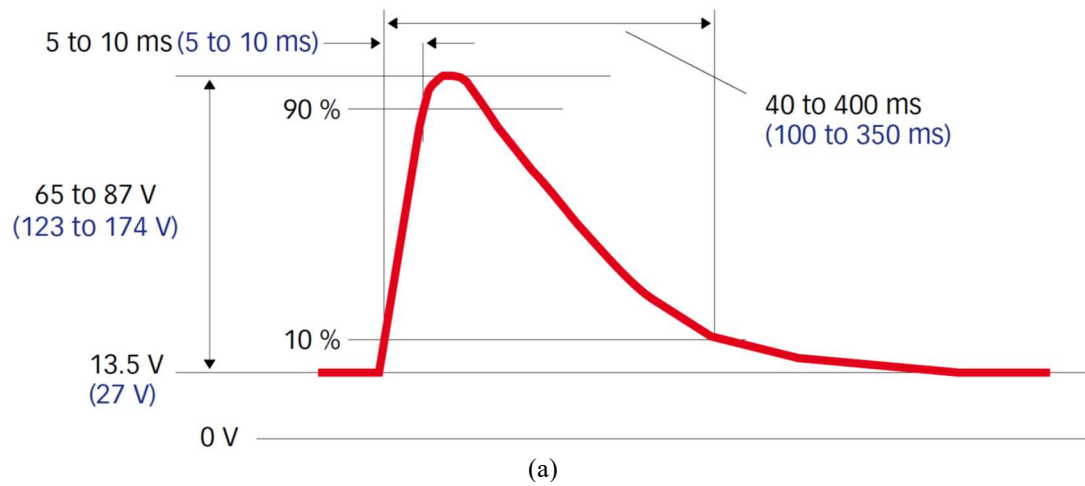


Figure B24: Load Dump Without (a) and With (b) Centralized Load Dump Suppression

Appendix C: Examples of Transient Stress Scenarios Beyond Standards

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C.1 Introduction

This appendix will highlight product-relevant cases of EOS. In WP4 on EOS [InCWP4], a categorization of root causes has been provided in the form of a fishbone diagram (see Figure C1). It differentiates between powered handling, unpowered handling, and AC operation-related failures. The key message is that understanding the system stress situation and quantifying the robustness of the exposed pin of a semiconductor device enables optimizing the board circuitry to manage the required stress level. This approach demands a deeper understanding of the actual stress applied to the system, which is typically induced from outside or from another part of the system, and of the propagation of that stress along various paths within the system. The most accurate method is the simulation of 3D electromagnetic behavior, which will be discussed later in the document, but it is often too complex to apply to real systems. However, even simplified analytical estimates will help eliminate incorrect system design decisions or missing critical threats to system components. Characterization methods and their use in system design decisions are discussed with examples. These include system ESD stress on LEDs, load dump stress on automotive parts, bus voltage (VBUS) related damage to USB interfaces, and several examples of failure mechanisms discussed in [InC2020].

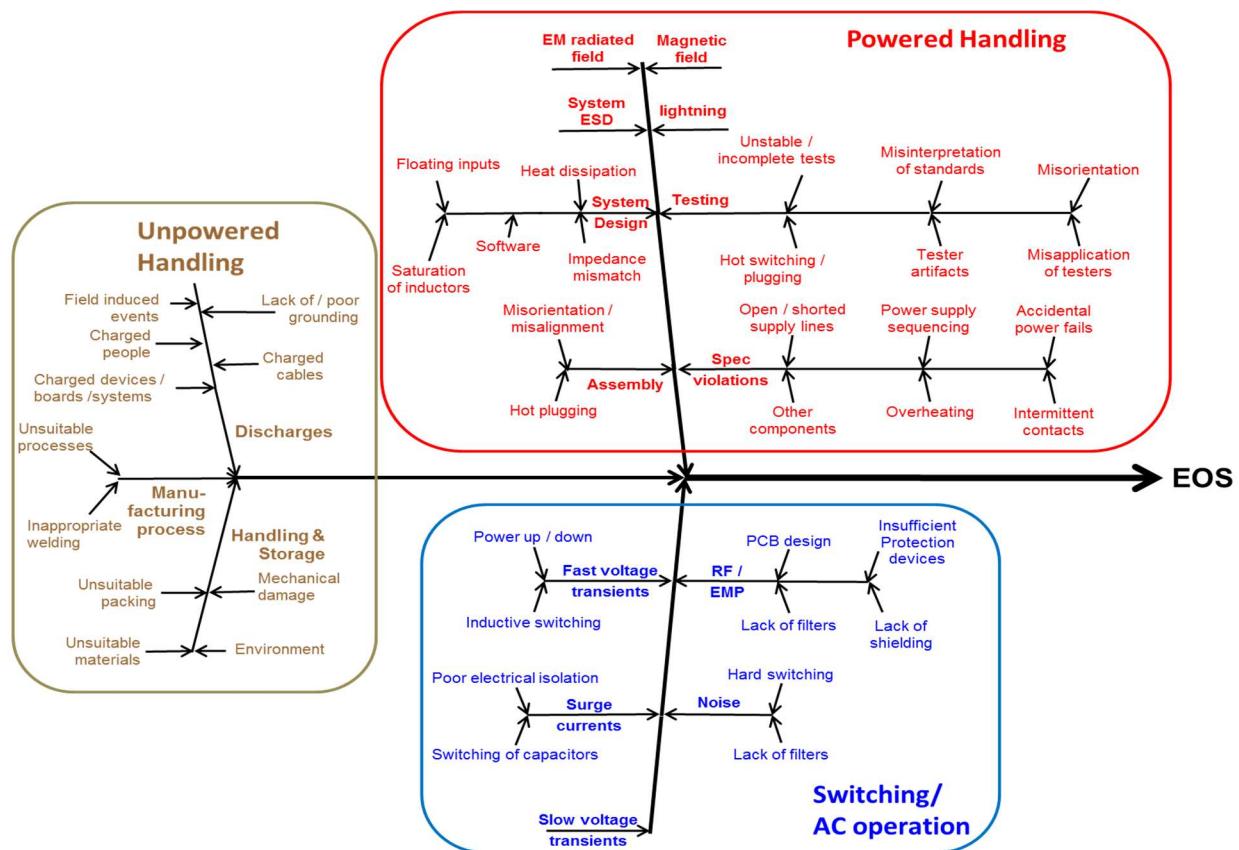


Figure C1: Fishbone Diagram of the Root Cause of Electrical Overstress (EOS) [InCWP4]

C.2 IEC 61000-4-2 [IEC6100042] and Real-World Stress of LEDs

Light-emitting diode (LED) junctions are notoriously vulnerable to ESD under reverse bias, via pins, or through discharges into the die due to plastic encapsulation breakdown. High-brightness LED (HB-LED) modules include many, sometimes dozens of LED junctions in large series-parallel arrays connected to a single pair of external electrodes labeled anode and cathode.

Normally, these HB-LEDs are very robust under forward-bias conditions, converting ESD energy into a brief flash of light. In reverse, however, they can distribute ESD energy unevenly, damaging some HB-LEDs and not others. This can result in minor changes in overall module brightness/leakage, which may or may not violate color and brightness specifications. In other words, there may be a “soft knee” of failure modes for these modules beyond their tAMR, which may or may not be detectable in certain applications.

Automotive system-level applications often include a series rectifier, current-limiting resistors, and a bypass capacitor. These all help protect the LED from automotive transients and reverse-battery-type testing, but also provide some ESD protection. A dedicated transient voltage suppressor (TVS) device in parallel with the LED and the current-limiting resistors (instead of, or in addition to, the series rectifier/bypass capacitance, if still desired) can properly protect the LED to a 30 kilovolt IEC 61000-4-2 test, which is essentially bulletproof in ESD terms.

LED manufacturers have included HBM TVS protection in parallel with HB modules, but the transient specification for ESD, much less for non-standard surge pulses, remains highly inconsistent across products.

C.3 Automotive ISO and High Voltage Device Failures

The supply of power to a vehicle is provided by two components: a battery and an alternator. The main function of the alternator is to convert mechanical energy into electrical energy in an alternating nature. When the combustion engine is running, the alternator rotates and generates alternating current (AC), which must be rectified. The vehicle's alternator generates electrical energy to charge the battery (see Figure C2).

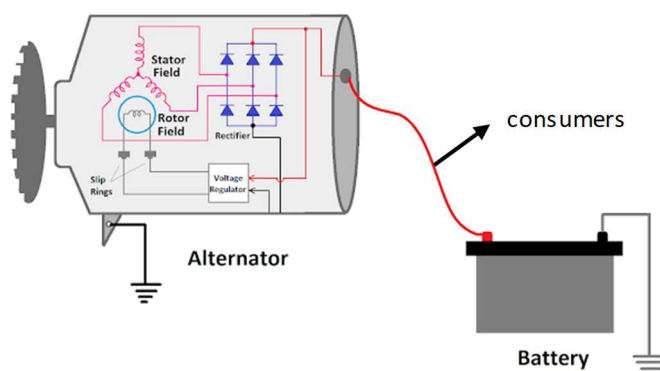


Figure C2: Alternator Wiring Diagram Including Connection to Battery and Consumers

During the vehicle operation, numerous consumers draw the electrical energy they need for their function from the corresponding pole of the battery. These include mechanical components such as starters and semiconductor-based applications.

A load dump event occurs when a powered load is disconnected. It can cause 2 problems:

- failure of supply to equipment or customers
- large voltage spikes from the inductive generator(s)

In automotive electronics, load dump refers to the disconnection of the vehicle battery from the alternator while the battery is being charged. This process of disconnecting occurs, for example, due to cable corrosion, poor connection, or during jump-starting. Due to such a battery disconnection, other loads connected to the alternator experience a voltage surge on the battery bus. This surge may reach 100+ volts and can take up to 400 ms to decay. In many (but not all!) vehicles, the surge is typically clamped through a so-called “central load-dump clamp” to 40 volts in 12-volt vehicles and about 60 volts in 24-volt systems. Depending on the availability of a central load-dump clamp in a vehicle, all consumers on the battery line must be secured against surges up to 40 volts (60 volts) or higher.

A typical semiconductor-based application that might be exposed to a load dump pulse, as described in Section B.2.2.3, is shown in Figure C3.

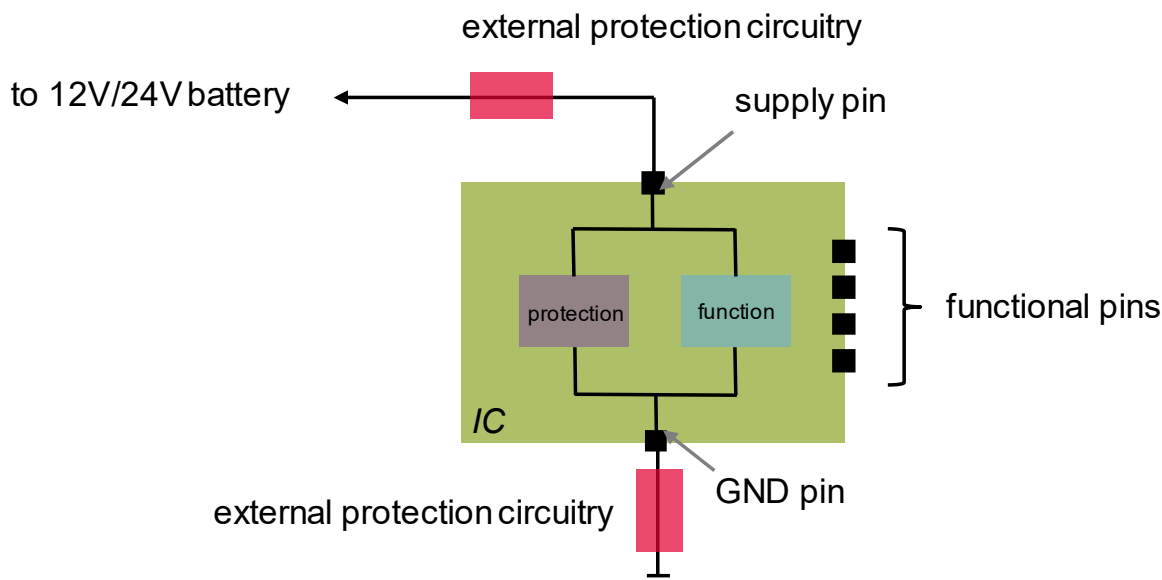


Figure C3: Simplified Representation of an IC Device Connecting the Supply and GND Pin to the Battery and GND System of the Vehicle

Note: To protect against a load dump, external devices, such as resistors, must be added on the supply or GND side of the device.

The IC device, for example, a sensor device or a switch, might be connected with its supply and GND pin to the battery or GND chassis of the vehicle.

The functional and protective (for example, ESD on the component level) parts of the internal circuit blocks need to be designed to remain functional during a load dump event. Section B.2.2.3 describes the load-dump parameters.

The main parameters are the pulse duration and the voltage amplitude, to which the battery voltage must then be added. Due to the low internal resistance of the source (a few ohms), the disturbance can be considered approximately an ideal voltage source.

Example for the modeling of a load dump situation:

- 13.2 volts (12 volts + 10%) + 86.5 volts = 99.7 volts for an unclamped load dump pulse in a 12-volt battery system
- t_d : 40 ms

Depending on the process technology used for the specific IC, the conditions for a load dump event may require additional protective measures, such as series resistors, in the application. Depending on the type of IC, such a resistor can be provided either in the supply (e.g., a sensor) or in the GND path (e.g., a high-side switch).

In the ideal case, neither the functional part of the circuit nor the ESD protective circuit, up to the targeted load dump voltage, exhibits significant breakdown behavior or reliability issues. Then no series resistor would be required. In all other cases, the ESD element and/or the functional circuit part must be considered using a power-to-fail analysis, for example, up to 40 ms (see above). The failure current information must then be used to dimension the series resistor accordingly.

C.4 VBUS Device Failure

Universal Serial Bus (USB) connectors are among the most common sources of EOS damage in communication devices. A malfunction at the VBUS pin, shorting to a neighboring IO pin, can cause severe EOS damage. According to the current USB Type-C power delivery specification, a maximum voltage of 20 volts can be applied to the VBUS line and connector pin. In the future, a maximum voltage of 50 volts is under consideration (this is by customer request to accommodate the noise on the supply line for a 48 V VBUS). In a failure case, the VBUS pin can come into contact with a nearby TX or RX pin, for example, by shorting out while pulling the cable out of the connector (see Figure C4). This results in a sudden discharge of the cable and the onboard buffer capacitance into the low-voltage IO circuitry of TX and RX (see Figure C5). To protect the IOs, AC caps are used, which provide the DC overvoltage protection. Nevertheless, a fast transient can occur during discharge, which is not blocked by the AC cap. The discharge of the onboard buffer caps in the μF regime can lead to several 10 A to 100 A over several 100 ns into the board network of the TX (see Figure C6). TVS diodes are used to mitigate this stress. Nevertheless, a stress of several tens of amps can occur at the IC pin if no series resistance is used. Typical values of a series resistance are in the range of 1-5 Ω . The performance of the high-speed interface limits the increase in the resistor value. A fundamental challenge of this discharge scenario is the lack of a standardized stress test.

The scenario can be reproduced in a SPICE simulation by assuming a low-impedance discharge caused by a metal-metal short. Using a system-efficient ESD design (SEED) type characterization of the IO behavior and the TVS diodes allows for optimizing the serial resistance and TVS diode selection. Knowledge of tAMR in the hundreds-of-ns range for the pin under study is needed to determine whether the simulated voltage, V_{TB} , is within a safe range.

Type C (enlarged)

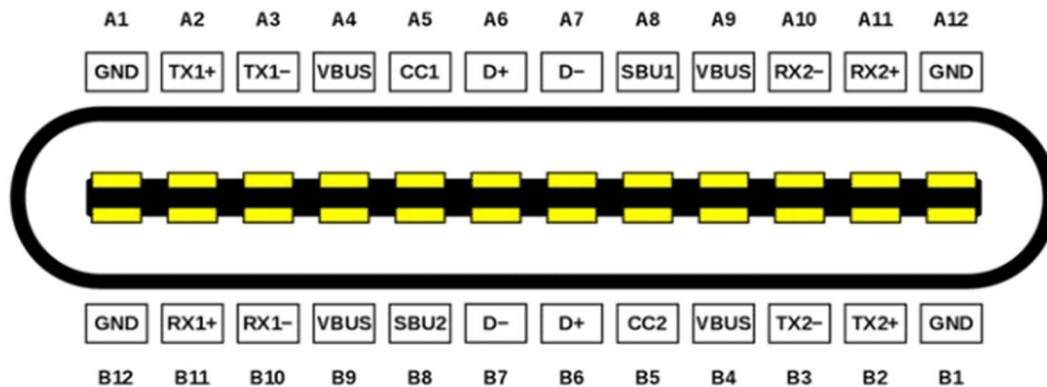


Figure C4: USB Type C Connector

• Problem Statement:

- VBUS can supply 20 V (recent requests up to 50 V)
- In a failure case, VBUS can be shorted at the port to the HS IO line
- No damage should occur at the HSIO pin (TX, TXRX, DP/DN) → safe design onboard protection

• Typical Stress Time Regime at IO Pins:

- In the range of tens to hundreds of nanoseconds

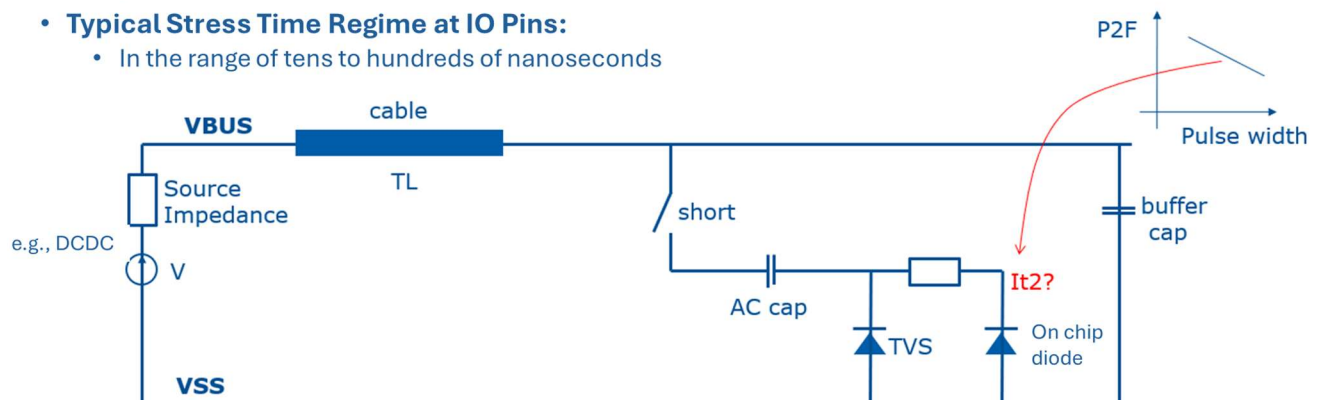


Figure C5: Discharge Scenario for a VBUS Short to TX/RX

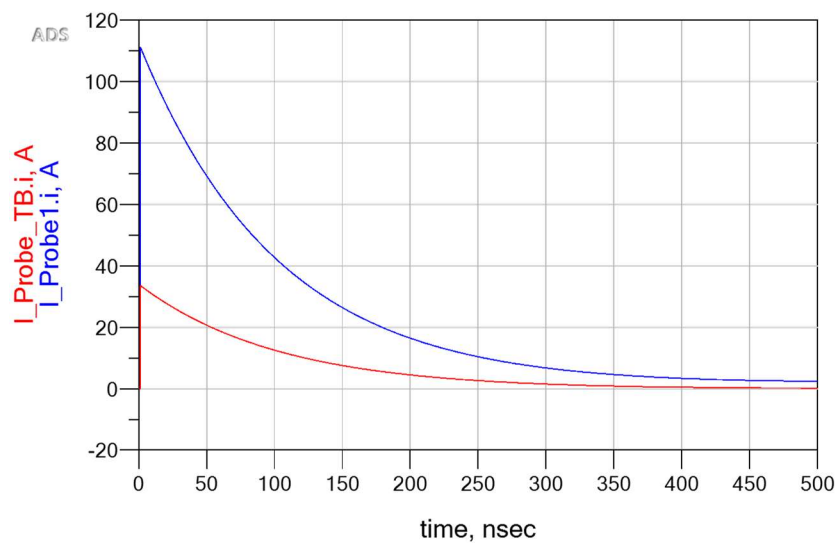
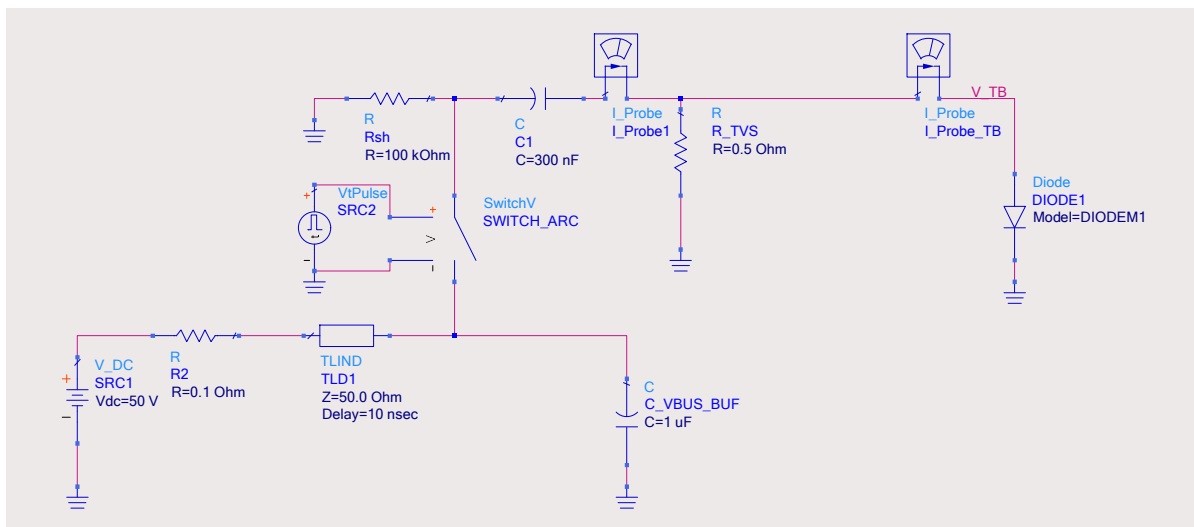


Figure C6: Simulation Deck for a VBUS Discharge (top) and Discharge Currents (bottom) Under Worst-Case Assumptions of a Short

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Revision History

Revision	Changes	Date of Release
1.0	Original release	October, 2026