Industry Survey Report

System Level – Direct PIN ESD

Industry Council on ESD Target Levels

February 2025

Revision 1.0

This document is available through various public domains as listed below:

The Industry Council on ESD

http://www.esdindustrycouncil.org/ic/en/

The Electrostatic Discharge Association

http://www.esda.org/

Abstract

- The read-out report addresses the feedback of the industry wide survey on system level direct pin ESD performed in the time frame of April to August 2024.
- The focus is on the status in industry and no recommendations are provided.
- The survey results show the usage of system level direct pin ESD in many application domains.
- It also highlights the lack of an aligned test procedure and target levels.

About the Industry Council on ESD Target Levels

The Council was initiated in 2006 after several major U.S., European, and Asian semiconductor companies joined to determine and recommend ESD target levels. The Council now consists of representatives from active full member companies and numerous associate members from various support companies. The total membership represents IC suppliers, contract manufacturers (CMs), electronic system manufacturers, OEMs, ESD tester manufacturers, ESD consultants and ESD IP companies. In terms of semiconductor market leaders 12 of the top 20 companies are members of the council.

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Mission Statement

The Industry Council on ESD Target Levels was founded on its original mission to review the ESD robustness requirements of modern IC products to allow safe handling and mounting in an ESD protected area. While accommodating both the capability of the manufacturing sites and the constraints posed by downscaled process technologies on practical protection designs, the Council provides a consolidated recommendation for future ESD target levels. The Council Members and Associates promote these recommended targets for adoption as company goals. Being an independent institution, the Council presents the results and supportive data to all interested standardization bodies.

In response to the growing prevalence of system level ESD and EOS issues, the Council has now expanded its mission to directly address one of the most critical underlying problems: insufficient communication and coordination between system designers (OEMs) and their IC providers. A key goal is to demonstrate and widely communicate that future success in building ESD robust systems will depend on adopting a consolidated approach to system design based on a clear and quantitative understanding of the IC robustness. To ensure a broad range of perspectives the Council has expanded its roster of Members and Associates to include OEMs as well as experts in system design and test.

Preface

The presented report is a summary of the findings of an industry wide survey on system level direct pin ESD (SL-DPE) which was performed by Industry Council on ESD Target Levels in the time frame from April to August 2024. The summary only targets the information about the industry feedback and doesn't imply any recommendation for test concepts or target levels.

Disclaimers

The Industry Council on ESD Target Levels is not affiliated with any standardization body and is not a working group associated with JEDEC, ESDA, JEITA, IEC, or AEC.

This document was compiled by recognized ESD experts from numerous semiconductor supplier companies, contract manufacturers and OEMs. The data represents information collected for the specific analysis presented here; no specific components or systems are identified.

The Industry Council, while providing this information, does not assume any liability or obligations for parties who do not follow proper ESD control measures.

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Glossary of Terms

CDM	Charged Device Model
EMC	ElectroMagnetic Compatibility
EFT	Electrical Fast Transient
ESD	ElectroStatic Discharge
EOS	Electrical OverStress
HMM	Human Metal Model
HBM	Human Body Model
PESD	Powered ESD
SL	System Level
SL-DPE	System Level - Direct Pin ESD
TLP	Transmission Line Pulsing

Executive Summary

The system level direct pin ESD survey has targeted the usage of stress pulses directly to system or subsystem pins of a system port (like USB). 54 responses have been received spreading across various industries including IC suppliers and IC (end)customers and geographies. Real-world failures are reported by 2/3 of the respondents. The predominant location for real world failures is at the customer site. A diverse spectrum of failure scenarios is observed.

System Level testing is most often done using IEC 61000-4-2 generators. Human metal model dominates the type of scenario to be reproduced (in contrast to cable discharge). The stress testing is very often a customer demand. The levels range from 2kV (or lower) to 15 kV without TVS and from 4 kV to > 15kV with TVS for almost all pin types which connect to a system pin. About 40% of the responses are reporting correlation between tested robustness and field returns. If correlation is not evident, it is mostly attributed to insufficient statistics and lack of information. 2/3 of the responses are considering SL-DPE as a design criterion. The design decisions are predominantly based on TLP results.

Introduction

1.1 System Level Direct Pin ESD (SL-DPE) industry survey

The term SL-DPE is coined for the stress testing of system port pins like a USB connector of a notebook computer by directly applying a type of ESD stress to one exposed pin of the connector. In most cases IEC 61000-4-2 ESD generators are used for this purpose. While the IEC 61000-4-2 standard itself excludes this type of stress testing if the connector has a grounded shield, this is, nevertheless, widely applied to characterize the robustness of a system interface. Due to the missing standard test practice and common protection design goals, there is often a misunderstanding and misalignment between IC supplier and system designer.

To get an overview of the usage across various industries and types of interfaces as well as the ways of testing and applied target levels, an industry-wide survey was conducted by the Industry Council on ESD Target Levels. The intention of this report is to give a comprehensive readout of the survey. At this point, it is not intended to be a white paper giving recommendations or proposing guidelines.

1.2 Survey Setup

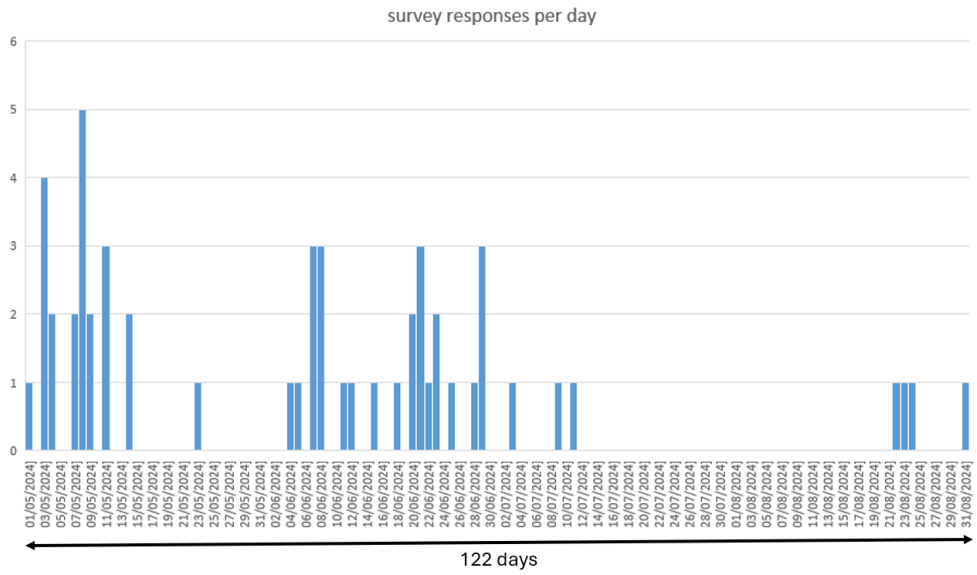
The industry survey was designed by the working group for System Level Direct Pin ESD (SL-DPE) of the Industry Council on ESD Target Levels. The answers were collected using Microsoft Forms and responses were recorded anonymously. The survey was launched at the end of April 2024 and was open until the end of August 2024.

A total of 32 questions were asked, either single-choice, multiple-choice, or text-based. The questionnaire could be completed leaving any number of questions unanswered. Answers left blank were ignored for the analysis. The percentages provided below are referring to how often a particular answer was given/selected as compared to total replies to a question – note, that for questions allowing to select multiple possible answers, the percentages of the individual answers are, hence, not adding up to 100. For reference, the full set of questions for the survey is shown in Appendix A1. Some of the answers given in text form have been paraphrased, and/or similar ones combined for the data presented.

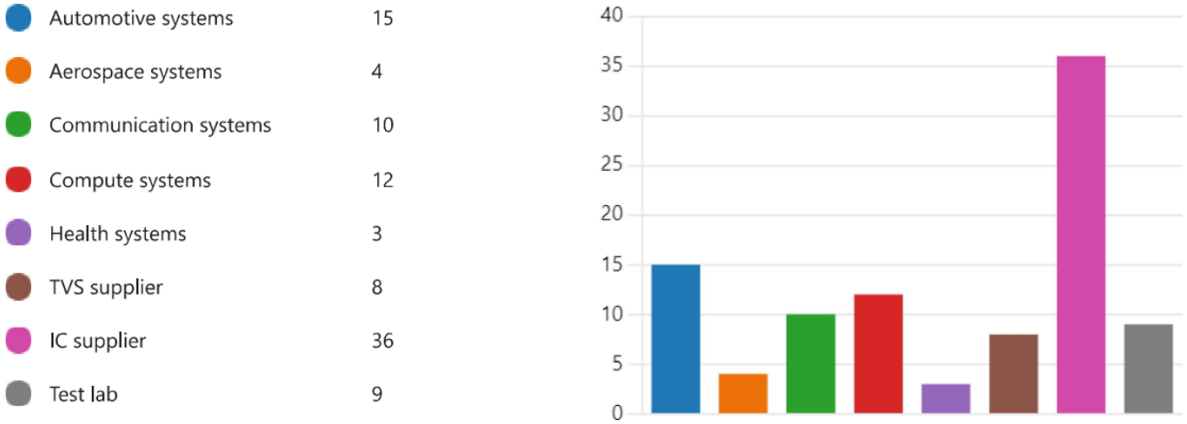
The questions and the corresponding responses can be organized into three categories: (1) real world failures (2), lab testing (3), targets & design. The report will follow this structure.

1.3 Participation

The survey was open from April to August 2024 and during that period a total of **54 responses** were submitted with the following distribution over time:



1. [Q01] Which industry or industries do you belong to? *(select all that apply)*

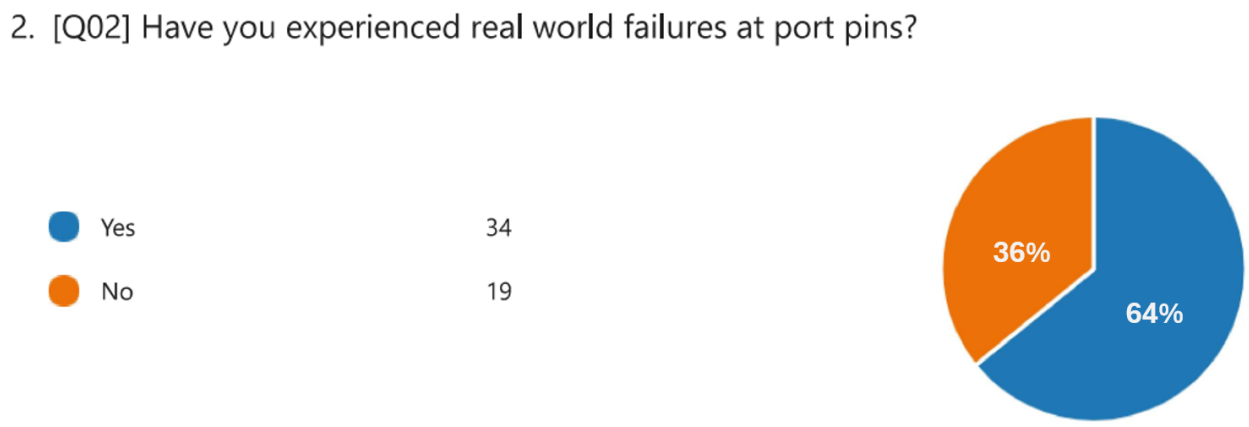


[Q1] 54 answers have been provided. Responses came from a wide range of industries, with *IC suppliers* being the dominating one. Several respondents identified as belonging to more than one category with one of them even selecting seven different options. Out of the 36 *IC supplier*-responses, only 20 identified merely as such while 16 selected further categories as well. For some of the questions below, the responses were also analyzed for *non-IC suppliers* and *IC suppliers* separately, where the latter then refers to all 36 responses mentioning *IC supplier* in question Q01.

Chapter 1: Real World Failures

Summary: There were some real-world failures reported, however, their interpretation is not always clear. The breakdown of these responses is examined below.

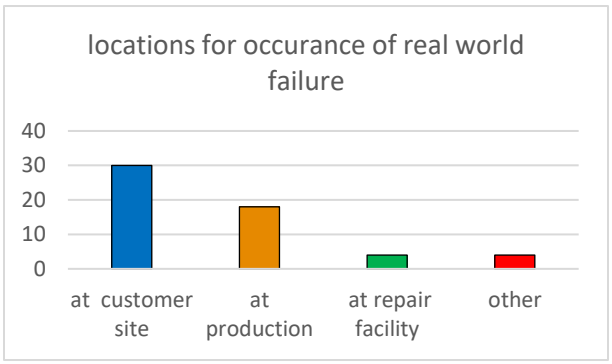
- ~2/3 have experienced real world failures
- Predominant location for real world failures is at customer site
- Diverse spectrum of failure scenarios with the following mentioned multiple times:
  - cable plugging events
  - testing at customer (also to pins with non system level (SL) robustness target)
  - too little information from customer
- 80% conduct failure analysis: mostly on-chip damage (thermal and dielectric breakdown)



[Q02] 53 answers have been provided. ~2/3 report that they have experienced real world failures at port pins. It should be noted that the term 'real world' was not further defined in the questionnaire and might carry different meanings for responders with different backgrounds. For IC manufacturers, it may refer to the company using the IC, which may be doing some EMC testing. For system designers, however, it may refer to the end customer. Comparing responses for *IC suppliers* vs. *non-IC suppliers*, shows a reported field failure rate of 61% and 71%, respectively.

3. [Q03] Where have real world failures occurred? *(select all that apply)*

At customer site	30	→ 88%
At production	18	→ 53%
At repair facility	4	→ 12%
Other	4	



For 'Other', the following answers were given

- *Certification lab*
- *At customer site, however, very little information is given back to us from our customers. Thus, the details of the failures are not there*
- *At customer system tests*
- *At IC customer site when doing testing or prototyping system*

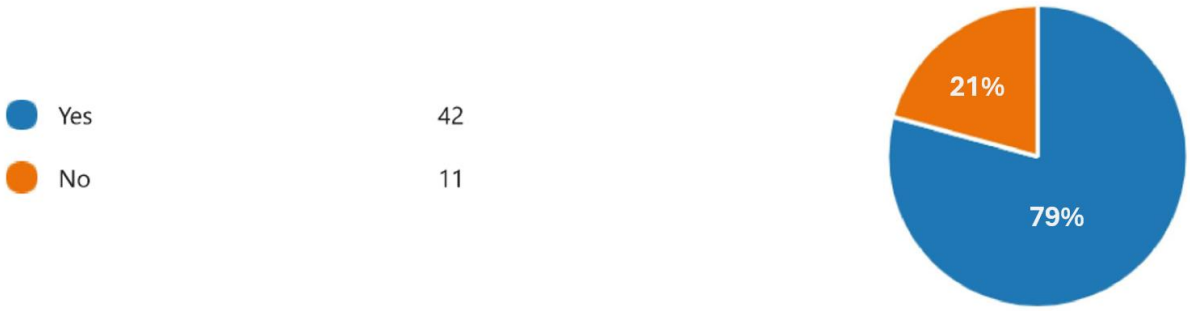
[Q03] 34 answers have been provided, aligning with the responses in the previous question Q02. Out of these, 88% reported the *customer site* as the location where real-world failures occur, followed by *at production* with 53%. For these two locations there is no notable difference between *IC suppliers* and *non-IC suppliers*. However, only *non-IC suppliers* report failures at *repair facilities*. 3/4 written responses for *others* could also be considered in the *customer site* category, further underlining it as the most common location for real world failures.

4. [Q04] Can you describe the real world failure scenario with a few words?

for detailed responses, see [Q04] in Appendix A2

[Q04] 32 answers have been provided. Overall, a broad spectrum of responses was provided describing scenarios at different levels of detail and scope. Two recurring trends were referring to *cable plugging* events as well as *testing at customer* sites. Also, there is frequent mention of insufficient availability of information from the customer.

5. [Q05] Do you do failure analysis?



[Q05] 53 answers have been provided. 42 out of these state that they conduct some sort of failure analysis. Notably, this is more than the 34 which responded in Q02 that they have experienced real world failures at port pins. In fact, 11 responses (9 out of them being *IC suppliers*) which selected *no* in Q02 did select *yes* for Q05 and only 3 that encountered failures according to Q02 do not carry out failure analysis. The reason for this mismatch is not clear but could be due to failures occurring during in-house testing before product release but after product release there were no field failures. However, it indicates that the prevalence of failures is even higher than reported in Q02.

6. [Q06] Can you describe the type of failure (thermal, dielectric breakdown,…) and the failure location (TVS diode, on board resistor,, on chip metal, input or output transistor,…)?

for detailed responses, see [Q06] in Appendix A2

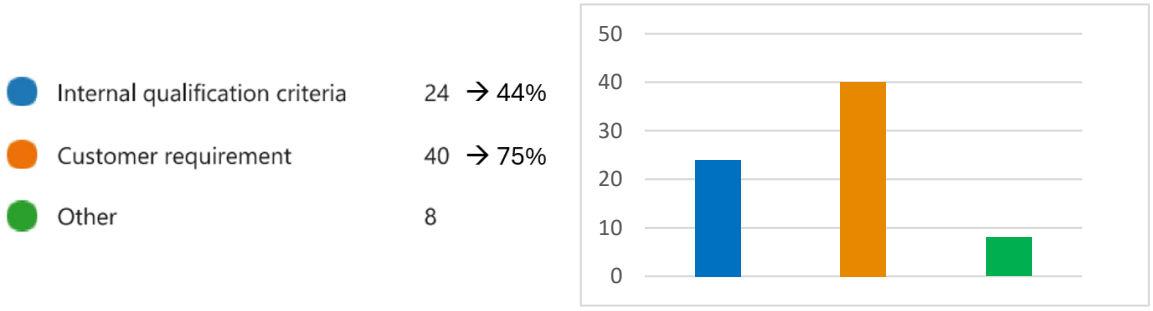
[Q06] 37 responses have been provided. Several failure types are described in the written responses, the two predominant ones being *dielectric breakdown* (15x) and *thermal damage* (22x). Most of the failures are reported to be on die and only a few (5x) are mentioning damage at board level. While many replies do not give details on the impacted structures, there are several mentioning damage of ESD components (11x) as well as one of insufficient ESD protection due to cost and performance. Notably, there is very little reporting of *soft fails* with only two mentions.

Chapter 2: Lab Testing

Summary:

- Most laboratories reported that Pin testing uses the IEC 61000-4-2 or closely related generators.
- Human metal model dominates the type of scenario to be reproduced (in contrast to cable discharge)
- To access the pins a wide variety of connection methods is used, from small pins to breakout boards and cables.
- The demand by a majority of customers justifies the need for SL-DPE

7. [Q07] Who is requiring System Level Direct PIN ESD (SL-DPE)? *(select all that apply)*

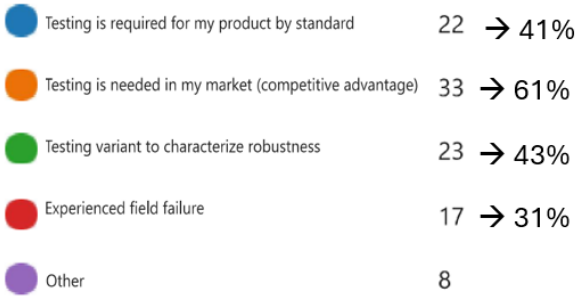


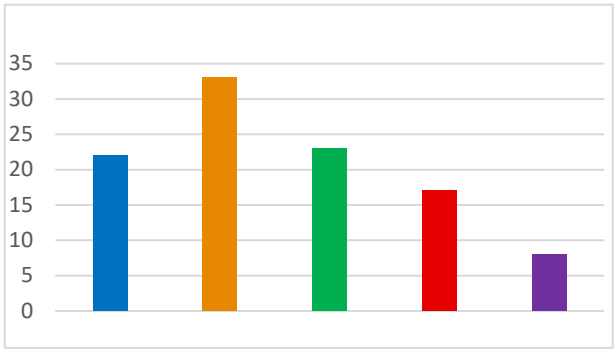
For 'Other', the following answers were given:

- *Need to be competitive with other vendors*
- *Would be good internal qualification control*
- *External qualification*
- *IEC documents for ICs (EMC context)*
- *Replicating Field Failures*
- *Industry standards for specific IC type/market;*
- *Nobody is requiring it (2x)*

[Q07] We received 54 responses, note that it was possible to select more than one reason. "Customer requirements" dominated with 75%. For non-IC suppliers, customer requirements still dominated with 67%, while internal qualification criteria rose from 39% (IC suppliers) to 56% (non-IC suppliers). A smaller group of other reasons, ranging from replicating field failures to nobody required it.

8. [Q08] Why do you apply or require SL-DPE? *(select all that apply)*



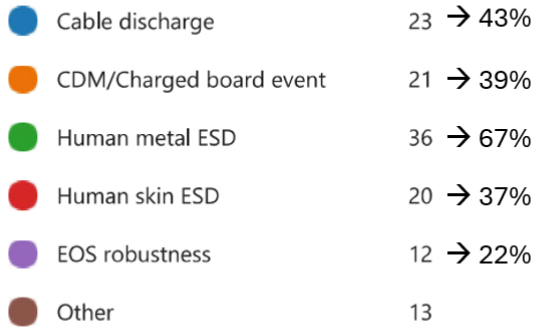


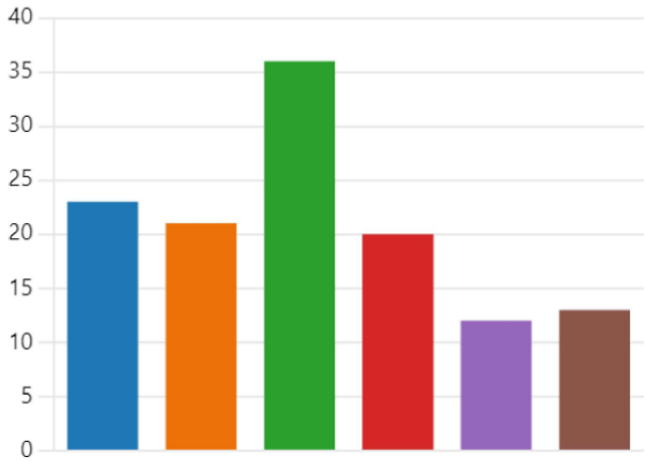
For 'Other', the following answers were given

- *Customer requirement (5x)*
- *Sometimes we characterize IC internal protection robustness using TLP*
- *Mapping of system-level ESD test scenario required by OEM to IC-level setup to support frontloading in overall Tier2 and Tier1 development flow*

[O08] 54 answers were provided. This question asks for more details about the motivation for SL-DPE testing. The most common motivation, 61%, is to gain a competitive advantage, but requirements and field failures also motivate testing, as well as ensuring quality by testing different variants.

9. [Q09] What stress type do you reproduce or try to reproduce? *(select all that apply)*





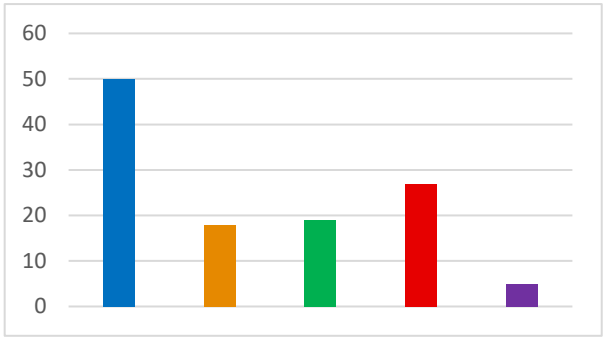
For 'Other', the following answers were given

- *IEC 61000-4-2 (3x)*
- *Customer requirement*
- *System level direct discharge (2x)*
- *IEC on an IC chip outside system*
- *EOS robustness (2x)*
- *Soft Error Immunity*
- *Active ESD directly on pins and stray field effects*
- *PESD, EFT*
- *Long pulse TLP, IEC gun (IEC could map somewhat to Human Metal ESD but doesn't follow SP5.6 in fixturing, just apply IEC gun)*
- *Unknow rootcause replicated by SL-DPE*
- *What is "EOS robustness" supposed to mean?*

[Q09] 54 answers were given. In these answers we again see the influence of the IEC 61000-4-2 standard: Human metal ESD, the basis for the waveforms in the standard, ranks first with 67%. This is followed by concerns about cable discharge at 43%, CDM and charged board events at 39%. Human skin ESD is usually less severe than human metal ESD. This is reflected in the data: 37% of respondents cited human skin ESD as opposed to 67% who cited human metal ESD.

10. [Q10] Which type of pulse generator do you use? *(select all that apply)*

IEC 61000-4-2	50 → 96%
HMM pulser	18 → 35%
ISO10605	19 → 37%
TLP	27 → 52%
Other	5

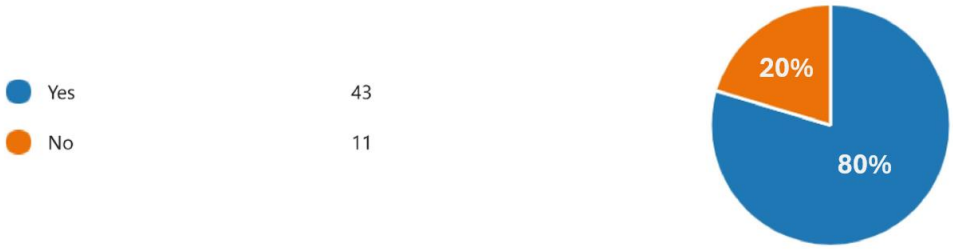


For 'Other', the following answers were given

- *Custom*
- *Stripline for field coupling*
- *Field Collapse Pulse (CBE-like)*
- *Surge*
- *What is the difference between "IEC 6100-4-2 pulser" and "ISO10605 pulser"?? The pulse is basically exactly the same, you have only the possibility to use also additional RC-network*

[Q10]. We received 52 responses. The IEC 61000-4-2 ESD generator dominated as the test instrument, with 96% of all responses including this generator. The similar ISO10506 generator is used by 37%, so generators that follow the IEC waveform dominate the choice of test generator, and the similar HMM waveform is used by 35%. The TLP, which produces clean and well reproducible waveforms, is used by 52% and the HMM pulse generator by 35% of the responses.

11. [Q11] Do you use an IEC61000-4-2 table set up (including standard coupling planes, grounding scheme, etc.)?



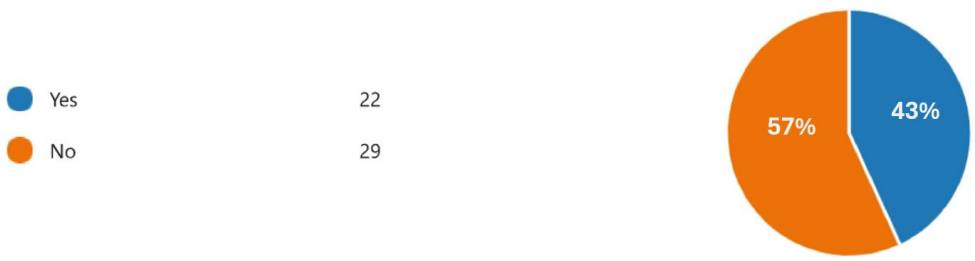
[Q11] We received 54 responses. The large majority of users of the IEC 61000-4-2 standard (43/50) apply the table set up for the system under test.

12. [Q12] What else do you follow for your setup?

for detailed responses, see [Q12] in Appendix A2

[Q12] 7 answers were provided. This question asks for further details about the test setup or methodology. Seven additional aspects were provided. Two replied that robotic test systems were used and some differences in the grounding of the coupling planes were noted in the survey responses.

13. [Q13] Do you use breakout boards/cables (for example to connect an ESD generator to a USB)?



[Q13] 51 answers have been provided. Breakout boards or cables can greatly change the stress seen by an IC. Within the 51 responses there is a rough split: 43% use breakout boards or cables, while 57% do not. The next questions ask for more details about the breakout boards or cables used. We did not ask why boards or cables were used and we cannot correlate this with the type of pins tested. However, it is reasonable to assume that some pins, such as USB pins, require the use of breakout boards or cables, as the small size of USB, DVI, etc. connectors means that it is not possible to touch connector pins with an ESD generator directly. On the other hand, it is easy to directly access large connector pins, such as those used in car engine controllers.

14. [Q14] Breakout boards - can you please describe?

for detailed responses, see [Q14] in Appendix A2

[Q14] We received 19 other details about breakout boards or cables. Some adapters are just short electrical connections such as "short cable connection", "only lead pin outside", "short cable adapter", "HDMI breakout board with exposed wires/test points", "pogo pin" and more complicated setups such as "evaluation board...", "PCB with minimal set of external components...", "... special PCB for robotic testing..." etc. The influence of the test fixture and the connection from the ESD generator to the system or IC under test can often determine the stress level. This requires further investigation.

15. [Q15] Breakout cables - can you please describe?

for detailed responses, see [Q15] in Appendix A2

[Q15] 17 answers have been provided. This question goes into more detail about breakout cables. As a wide variety of cables are briefly mentioned, the only conclusion that can be drawn is that the injection mechanism is uncontrolled, although it can have a strong effect on the stress level applied.

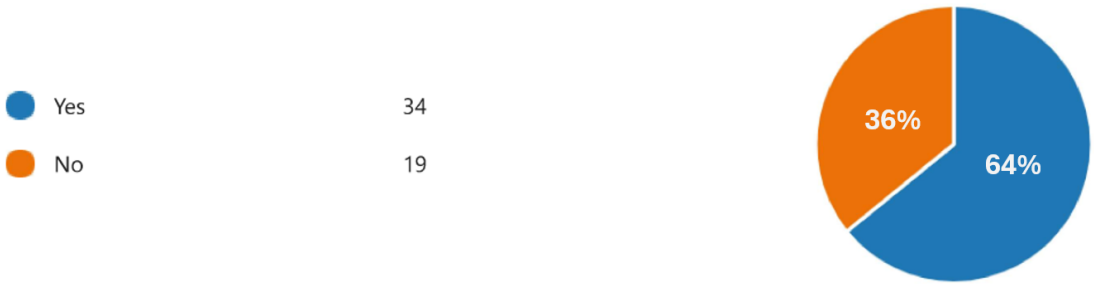
16. [Q16] Which discharge mode do you employ in your methodology? *(select all that apply)*

[Q16] We received 53 responses. All respondents use the contact mode and 47% also use the air discharge mode. Contact discharge includes IEC testing as well as alternatives like HMM.

17. [Q17] What kind of failures do you monitor in the SL-DPE testing? *(select all that apply)*

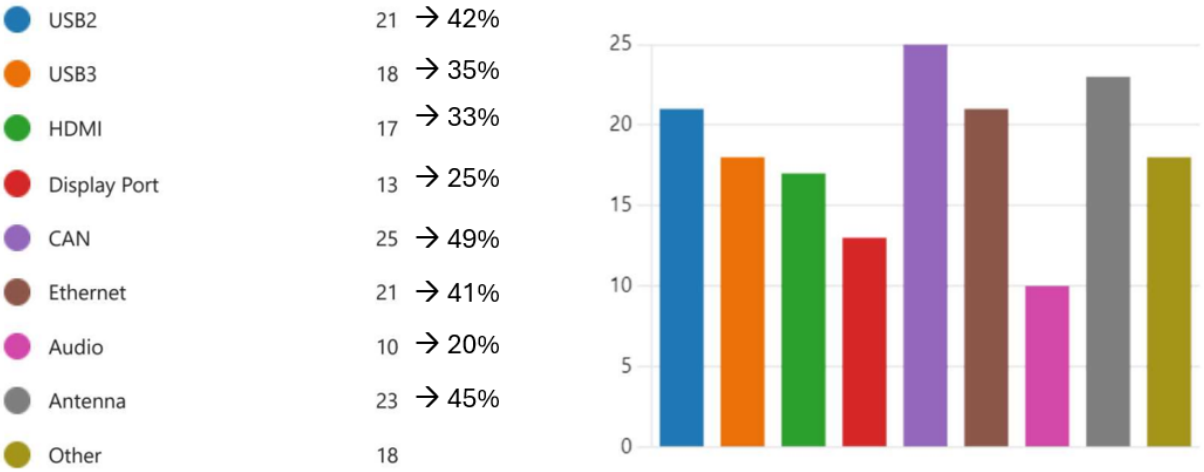
[Q17] Again, we received 53 responses. Pretty much all, 96%, observe damage, while 64% observe soft failures in addition to damage. In order to observe soft failures, the system under test must be powered up and operating. Such a powered system tests cannot be performed on a standalone IC.

18. [Q18] Do you rate System Level Direct Pin ESD (SL-DPE) as repeatable?



[Q18] All 53 respondents answered this question. Most, 64%, consider SL-DPE to be repeatable.

19. [Q019] Which ports are tested?



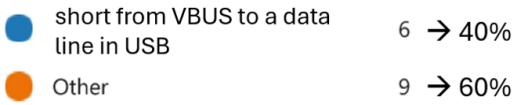
For 'Other', the following answers were given

- *LIN (7x)*
- *Mobile display connector pins*
- *PCIe*
- *Special ports*
- *Input wrist strap and smock, I/O ports*
- *Global IOs pins for automotive products*
- *Supply, wake, high side switches, custom interfaces, etc.*
- *PoE*
- *I2C*
- *legacy automotive interfaces (SENT, PSI, LIN), general purpose global IOs, global supply pins*

- *BAT/Wake*
- *all pins of an MCU or MPU*
- *PSI5*
- *PSI and other customized inputs and outputs*
- *RSxxx*

[Q19] 51 answers were provided. Based on these responses, we see a wide range of ports being tested. Most of the ports are externally accessible by a customer. Testing mainly high-speed and RF ports seems reasonable, as it is relatively easy to protect low-speed and power connections.

26. [Q26] Have you developed a test for other pin stress scenarios? *(select all that apply)*



For 'Other', the following answers were given

- *No (4x)*
- *Surge test*
- *Sensor Pins*
- *We recently have requests to do powered on TLP and powered on VF-TLP and to correlate that to an IEC failure level (which the two do not correlate but we get these requests anyway)*
- *Field Collapse Pulse (charged board discharge through IO)*
- *During development, various non-standard tests are developed on the basis of the problem situation*

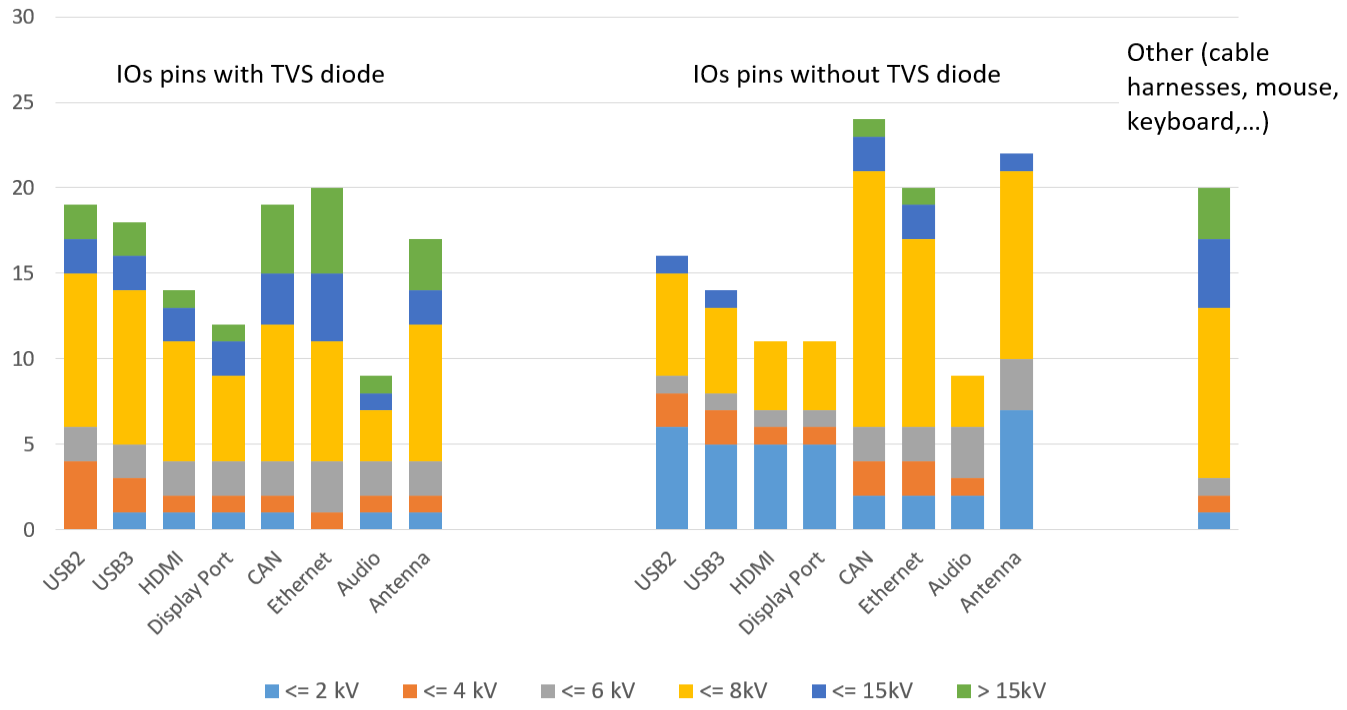
[Q26] 15 answers were provided. These included 6 responses referring to a test of a VBUS short to data line. Various other tests included powered TLP and surge tests. Besides the USB VBUS test, there doesn't appear any broader significance of a specific stress test.

Chapter 3: Qualification/Testing Targets and Design Goals

Summary (the following overview lists observations from different industries and do not constitute recommendations):

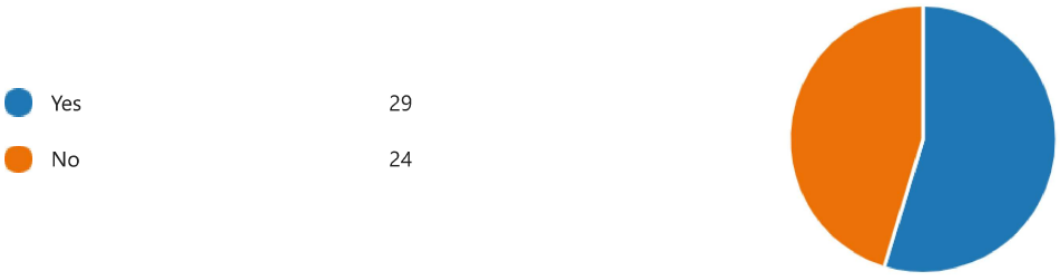
- Only 50% of responses provide detailed feedback on targets per interface for system level direct ESD pin testing.
- The reported levels range from 2 kV (or lower) to 15 kV without TVS and from 4 kV to >15 kV with TVS for almost all pin types which connect to a system pin.
- Exceptions are CAN and Ethernet pins where a higher ESD robustness is expected without TVS devices.
- About 40% of the response are reporting correlation between tested robustness and field returns. If there is missing corelation it is mostly attributed to insufficient statistics and lack of information.
- 2/3 of the responses are considering SL-DPE as a design criterion. The design decisions are predominantly based on TLP results.

20. [Q20] What target levels do you apply for each of the following interfaces (contact discharge)?



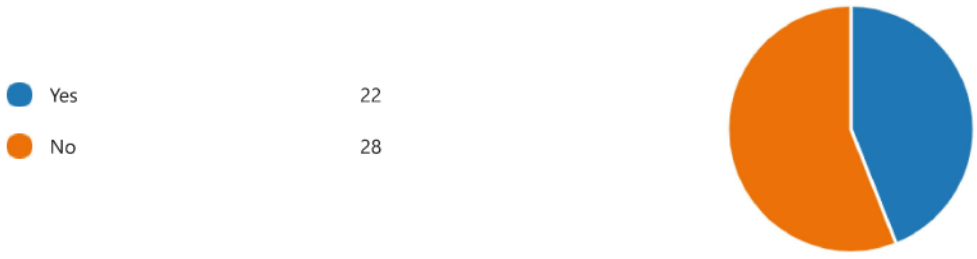
[Q20] Depending on the IO type 18 - 24 answers have been provided (“n/a” responses have been omitted). Not all responses have addressed all types of IOs. It is clearly seen that there is both a lack of test targets, and the targets vary considerably between companies. It is obvious that the largest target group is a goal of 8 kV. This can probably be traced back to the standards like CE where a contact ESD robustness of a system of 8 kV is requested. In these cases, there is no distinction between a chassis part and a port connector, despite the exclusion of the system level direct pin ESD test by IEC 61000-4-2 in case of connectors with grounded shield. Only 7 of the respondents have different target levels for testing w/ and w/o a TVS diode. All 7 of these respondents identify themselves also as system manufacturers.

21. [Q21] Do you also test supply pins for these interfaces?



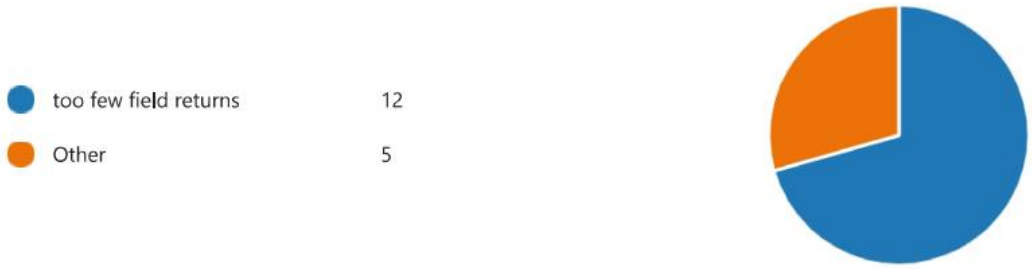
[Q21] 53 answers have been provided. 29/53 apply system level direct pin ESD stress also to the supply pins.

22. [Q22] Do you see any correlation between the robustness of the pins evaluated by your applied direct pin stress test method and field returns?



[Q22] 50 answers have been provided. From the group of IC suppliers 14/33 (42%) have answered with yes. From the group of non- IC suppliers 8/17 (47%) have confirmed a correlation. Less than half of the companies see a correlation between the robustness of the part evaluated by the type of test they apply and the field returns. Given the complexity of analyzing the correlation across a supply chain in very different industrial domains and markets, it is not surprising that the correlation between the measured robustness and field returns is <50%.

23. [Q23] Can you give details on missing correlation to field returns? *(select all that apply)*



[Q23] 17 answers have been provided. IC suppliers 6/9 (67%) and Non-IC suppliers 6/8 (75%) claim too few field returns to create a meaningful correlation.

For 'Other', the following answers were given

- *No detailed FA*
- *too little information from the field*

In some cases, an EOS type field fails were suspected:

- *ESD Requirement at good level*
- *Hard to assess if returned devices damages are due to ESD or EOS*
- *Customer did not comply with our IC usage guidelines, including power-up sequence, max rating ...etc*

24. [Q24] What are the field scenarios for which you observed correlations?

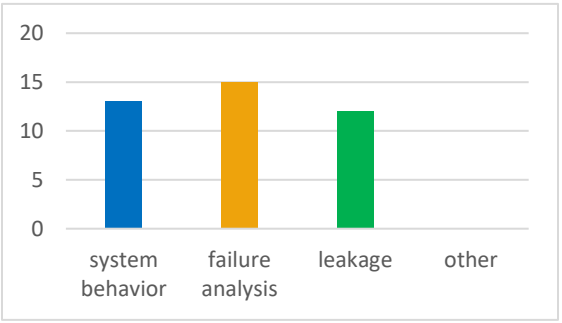
for detailed responses, see [Q24] in Appendix A2

[Q24] 18 answers have been provided. Systems with low ESD robustness as tested in the lab or low-cost systems without ESD protection on the board show higher field return rate. On the contrary, if passing internal system ESD tests, no ESD related field return is seen. Correlation was found to poor ESD

protection methods in the environment or to weak system design. For example, the wiring of IC pins to an exposed part of the system. Hot plugging and cable discharge are also mentioned as discharge scenarios in the field. A Damage of antenna and USB interfaces are explicitly quoted as reasons for field fails.

25. [Q25] What were the criteria for the observed correlations to field returns? *(select all that apply)*

system behavior	13	→ 56%
failure analysis	15	→ 65%
leakage	12	→ 52%
Other	0	



[Q25] 22 answers have been provided. The question has only addressed the group of responses who are claiming correlation. The response was analysed for IC supplier and non-IC suppliers. Multiple answers were possible (e.g. leakage and system behaviour were considered in the correlation).

IC suppliers

- system behavior 10/15 → 67%
- failure analysis 7/15 → 47%
- leakage 9/15 → 60%
- other 0/15 → 0%

Non-IC suppliers

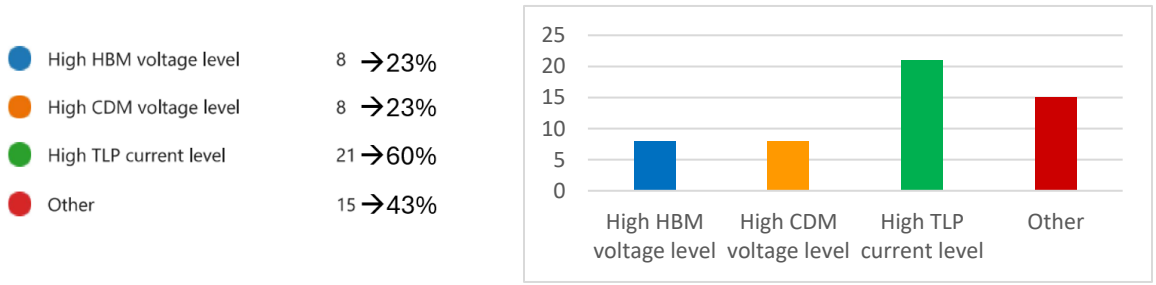
- system behavior 3/8 → 38%
- failure analysis 8/8 → 100%
- leakage 3/8 → 38%
- other 0/8 → 0%

It is an interesting fact that IC suppliers have a higher focus on system behavior, while non-IC suppliers are basing their judgement on physical failure analysis. Overall, it can be stated that system behavior, failure analysis and leakage testing are considered in the evaluation.

27. [Q27] Do you consider System Level Direct Pin ESD (SL-DPE) as a design criterion for IC design or IO IP design?

[Q27] 49 answers have been provided. 23 of 33 responding with yes are IC suppliers. These are 64% (23/36) of all responses identifying themselves to be IC suppliers (see [Q01]).

28. [Q28] What is the design criterion of the IC interface to achieve high robustness under system level direct pin ESD conditions? Design for ... *(select all that apply)*



For 'Other', the following answers were given

- *TLP current target & high TLP Clamp voltage*
- *Long(er) pulses*
- *Passing IEC61000-4-2 or ISO 10605 stress*
- *High IEC 61000-4-2 at IC level*
- *System ESD stress pulse (with or without PCB components depending on pin category)*
- *8kV pass with IEC gun on IC outside the system*
- *Residual current on chip as expected from SEED simulation with application; expected transient voltage at pin under test and supply and GND*
- *PESD direct pin discharge*
- *Direct application of HMM*
- *Appropriate optimization with SEED*
- *Simulations*

[Q28] 35 answers have been provided. Only 6/35 base their decision on HBM or CDM or IEC system level testing only. Others include some form of TLP testing, often combined with CDM/HBM testing, to make a design decision.

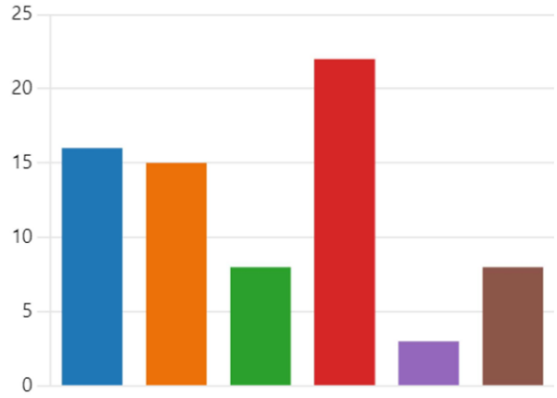
29. [29] Can you provide details on the higher target levels for the IC interface?

for detailed responses, see [Q29] in Appendix A2

[Q29] 26 answers have been provided. It is mentioned that higher levels are driven by system customers or competition. Test to fail are requested to evaluate headroom. Typical high robustness level interfaces are LIN, PSI5 and USB. The system testing can be performed by ISO 10605 and IEC 61000-4-2. Levels of 4 kV to 15 kV contact (and even 25 kV air) discharge are targeted. A pin specific design target of 2 A @50 ns TLP is mentioned for the stand-alone IC. Others require 30 A @ 100 ns TLP at the port pin. Chip/board codesign is seen as most cost efficient, but higher protection on silicon can be easier for system integration and more compact board design. SEED methodology is applied in some cases.

30. [Q30] How does your company allocate responsibility for *setting* goals and *managing* System ESD Robustness Qualification (IEC levels, test points, failure criteria, qualification failures)? *(select all that apply)*

Centralized responsibility for all ESD issues (factory, component, and system levels)	16	→43%
Product Engineer assesses system ESD levels required (from minimums or internal product application specs)	15	→41%
PCBA Designer assesses system ESD levels required (from minimums or internal product application specs)	8	→22%
Internal EMC/ESD Specialist/Group assesses system ESD levels required (from minimums or internal product application specs)	22	→59%
External EMC/ESD Specialist (consultant or 3rd party test/measurement)	3	→8%
Other	8	



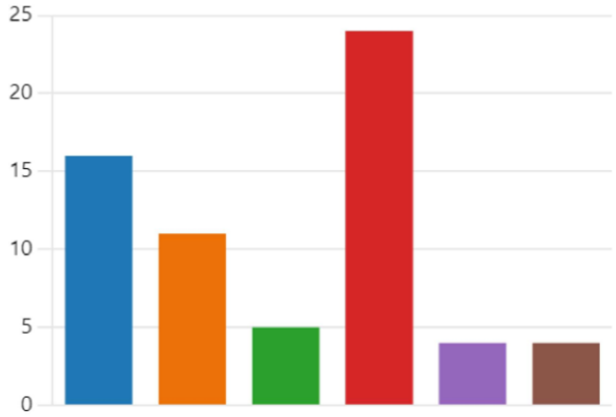
For 'Other', the following answers were given (each 1x)

- *Rely on individual manufacturer of the product*
- *integral along the whole chain S-2020; all vendors involved*
- *Product definer in contact with customers*
- *Design Engineer*
- *Envelope targets derived from OEM requirements*
- *System & Application Engineering*
- *Quality and Marketing teams*
- *Applications*

[Q30] 37 answers have been provided. The system level ESD targets are predominantly defined and monitored by corporate EMC experts or by product engineers. The PCB design has less influence on the system level ESD targets.

31. [Q31] How does your company allocate responsibility for *design measures* to achieve System ESD Robustness Goals (protection device/shielding selection decisions, simulation/validation)? *(select all that apply)*

Centralized responsibility for all ESD issues (factory, component, and system levels)	16 →55%
Product Engineer assures system ESD robustness (recommends circuit protections/shielding to PCBA Designer)	11 →38%
PCBA Designer assures system ESD robustness (determines and implements circuit protections/shielding independently)	5 →17%
Internal EMC/ESD Specialist/Group assures system ESD robustness (recommends circuit protections/shielding to PCBA Designer)	24 →83%
External EMC/ESD Specialist assures system ESD robustness (recommends circuit protections/shielding to PCBA Designer)	4 →14%
Other	4



For 'Other', the following answers were given (each 1x)

- *Rely on the individual component/assembly manufacturer*
- *Design Engineering/Vendor Suggestions*
- *Application engineer experience with IEC testing and what shunt inductor values will help pass 8kV contact discharge on the IC outside the system*
- *Co-development of system and IC-design (ASICs)*

[Q31] 31 answers have been provided. The same groups defining the targets are also directly involved in finding design solutions. The EMC experts are the key decision makers for the design measures.

32. [Q32] Any other comment you want to add?

for detailed responses, see [Q32] in Appendix A2

Summary and Outlook

The survey has shown a significant usage of system level direct pin ESD, mostly applying an IEC 61000-4-2 generator, in industry, while IEC 61000-4-2 typically excludes stressing port pins (with the exception of unshielded ports). There is neither a unique testing method nor common test target levels reported. This leads to a large ambiguity and a waste of effort and time in industry. The Industry Council will explore the support by industry to get consolidated recommendations.

Appendix A:

A.1 Questionnaire

1. [Q01] Which industry or industries do you belong to? *(select all that apply)*

- [ ] Automotive systems
- [ ] Aerospace systems
- [ ] Communication systems
- [ ] Compute systems
- [ ] Health systems
- [ ] TVS supplier
- [ ] IC supplier
- [ ] Test lab

2. [Q02] Have you experienced real world failures at port pins?

- ◯ Yes
- ◯ No

3. [Q03] Where have real world failures occurred? *(select all that apply)*

- [ ] At customer site
- [ ] At production
- [ ] At repair facility
- [ ] Other

4. [Q04] Can you describe the real world failure scenario with a few words?

5. [Q05] Do you do failure analysis?

- ◯ Yes
- ◯ No

673

6. [Q06] Can you describe the type of failure (thermal, dielectric breakdown,...) and the failure location (TVS diode, on board resistor,, on chip metal, input or output transistor,...)?

674

7. [Q07] Who is requiring System Level Direct PIN ESD (SL-DPE)? *(select all that apply)*

- ☐ Internal qualification criteria
- ☐ Customer requirement
- ☐ Other

675

8. [Q08] Why do you apply or require SL-DPE? *(select all that apply)*

- ☐ Testing is required for my product by standard
- ☐ Testing is needed in my market (competitive advantage)
- ☐ Testing variant to characterize robustness
- ☐ Experienced field failure
- ☐ Other

676

9. [Q09] What stress type do you reproduce or try to reproduce? *(select all that apply)*

- [ ] Cable discharge
- [ ] CDM/Charged board event
- [ ] Human metal ESD
- [ ] Human skin ESD
- [ ] EOS robustness
- [ ] Other

677

10. [Q10] Which type of pulse generator do you use? *(select all that apply)*

- [ ] IEC 61000-4-2
- [ ] HMM pulser
- [ ] ISO10605
- [ ] TLP
- [ ] Other

678

11. [Q11] Do you use an IEC61000-4-2 table set up (including standard coupling planes, grounding scheme, etc.)?

- ◯ Yes
- ◯ No

679

12. [Q12] What else do you follow for your setup?

680

13. [Q13] Do you use breakout boards/cables (for example to connect an ESD generator to a USB)?

- ◯ Yes
- ◯ No

681

14. [Q14] Breakout boards - can you please describe?

15. [Q15] Breakout cables - can you please describe?

16. [Q16] Which discharge mode do you employ in your methodology? *(select all that apply)*

- [ ] Air discharge
- [ ] Contact discharge

17. [Q17] What kind of failures do you monitor in the SL-DPE testing? *(select all that apply)*

- [ ] Damage
- [ ] Soft failure

18. [Q18] Do you rate System Level Direct Pin ESD (SL-DPE) as repeatable?

- ◯ Yes
- ◯ No

19. [Q019] Which ports are tested?

- [ ] USB2
- [ ] USB3
- [ ] HDMI
- [ ] Display Port
- [ ] CAN
- [ ] Ethernet
- [ ] Audio
- [ ] Antenna
- [ ] Other

20. [Q20] What target levels do you apply for each of the following interfaces (contact discharge)?

	<= 2 kV	<= 4 kV	<= 6 kV	<= 8kV	<= 15kV	> 15kV	n/a
USB2 - IO pin with TVS	○	○	○	○	○	○	○
USB2 - IO pin without TVS	○	○	○	○	○	○	○
USB3 - IO pin with TVS	○	○	○	○	○	○	○
USB3 - IO pin without TVS	○	○	○	○	○	○	○
HDMI - IO pin with TVS	○	○	○	○	○	○	○
HDMI - IO pin without TVS	○	○	○	○	○	○	○
Display Port - IO pin with TVS	○	○	○	○	○	○	○
Display Port - IO pin without TVS	○	○	○	○	○	○	○
CAN - IO pin with TVS	○	○	○	○	○	○	○
CAN - IO pin without TVS	○	○	○	○	○	○	○
Ethernet - IO pin with TVS	○	○	○	○	○	○	○
Ethernet - IO pin without TVS	○	○	○	○	○	○	○
Audio - IO pin with TVS	○	○	○	○	○	○	○
Audio - IO pin without TVS	○	○	○	○	○	○	○
Antenna - IO pin with TVS	○	○	○	○	○	○	○
Antenna - IO pin without TVS	○	○	○	○	○	○	○
Other (like cable harnesses, mouse, keyboard,...)	○	○	○	○	○	○	○

21. [Q21] Do you also test supply pins for these interfaces?

- ◯ Yes
- ◯ No

22. [Q22] Do you see any correlation between the robustness of the pins evaluated by your applied direct pin stress test method and field returns?

- ◯ Yes
- ◯ No

23. [Q23] Can you give details on missing correlation to field returns? *(select all that apply)*

- ☐ too few field returns
- ☐ Other

24. [Q24] What are the field scenarios for which you observed correlations?

25. [Q25] What were the criteria for the observed correlations to field returns? *(select all that apply)*

- ☐ system behavior
- ☐ failure analysis
- ☐ leakage
- ☐ Other

26. [Q26] Have you developed a test for other pin stress scenarios? *(select all that apply)*

- ☐ short from VBUS to a data line in USB
- ☐ Other

27. [Q27] Do you consider System Level Direct Pin ESD (SL-DPE) as a design criterion for IC design or IO IP design?

- ◯ Yes
- ◯ No

28. [Q28] What is the design criterion of the IC interface to achieve high robustness under system level direct pin ESD conditions? Design for ... *(select all that apply)*

- [ ] High HBM voltage level
- [ ] High CDM voltage level
- [ ] High TLP current level
- [ ] Other

29. [29] Can you provide details on the higher target levels for the IC interface?

30. [Q30] How does your company allocate responsibility for *setting* goals and *managing* System ESD Robustness Qualification (IEC levels, test points, failure criteria, qualification failures)? *(select all that apply)*

- [ ] Centralized responsibility for all ESD issues (factory, component, and system levels)
- [ ] Product Engineer assesses system ESD levels required (from minimums or internal product application specs)
- [ ] PCBA Designer assesses system ESD levels required (from minimums or internal product application specs)
- [ ] Internal EMC/ESD Specialist/Group assesses system ESD levels required (from minimums or internal product application specs)
- [ ] External EMC/ESD Specialist (consultant or 3rd party test/measurement)
- [ ] Other

31. [Q31] How does your company allocate responsibility for *design measures* to achieve System ESD Robustness Goals (protection device/shielding selection decisions, simulation/validation)? *(select all that apply)*

- [ ] Centralized responsibility for all ESD issues (factory, component, and system levels)
- [ ] Product Engineer assures system ESD robustness (recommends circuit protections/shielding to PCBA Designer)
- [ ] PCBA Designer assures system ESD robustness (determines and implements circuit protections/shielding independently)
- [ ] Internal EMC/ESD Specialist/Group assures system ESD robustness (recommends circuit protections/shielding to PCBA Designer)
- [ ] External EMC/ESD Specialist assures system ESD robustness (recommends circuit protections/shielding to PCBA Designer)
- [ ] Other

32. [Q32] Any other comment you want to add?

33. [Q33] If you would like to receive a copy of the final report, please provide an e-mail address to which it should be sent

A.2 Detailed responses to text questions

[Q04] Can you describe the real world failure scenario with a few words?

- Human touching, module charging
- Failure happened during function tests at customer site
- System Malfunctioning
- When installing electronic products into test equipment. When connecting a probe module to analyze or update electronics.
- The input buffers fail, cannot amplify the signal.
- Plug in process and uncontrolled chassis metal touch
- Mostly, non-intended externally accessible pins had been made accessible: power, oscillator, interrupt
- Users real touches, Ungrounded repair
- we meed real world failure from custom, it seems like ESD stress from failure analysis, but we don't know failure scenario how ESD stressed into these pins in custom environment.
- Plug and unplug the cable
- a broken capMIM at antenna pin
- Discharge with cable during plugging.
- Failure because of repetitive testing in one polarity on customer's side.
- Charged human plugging in a cable to tester, damaging input I/O.
- Test engineer at customer placed tip of tester into antenna port connector on phone mainboard and pulled the trigger. Test to test angle of the stress probe varied. Also board discharge between stress events was inconsistent. Voltage was incremented until the system failed.
- At production line of Tier1 and OEM.
- Mainly during manufacturing at OEM (especially car OEM assembly line with improper ESD concept), very seldomly fails at customer which have been mechanical problems (wrong construction)
- 1) Chaged soldering iron discharges to IC pins, 2) Reverse Polarity Bootleg Ground in damaging HDMI ports, 3) Etc

- I have observed pin failures during testing as well as in real life use on PoE ports. The damage occurs typically to the MOSFETS in the bridge rectifier on the VDD and VSS power nets of the PoE ports. The failure occurs during plugging in of cable in real world or during an ESD test if discharge is performed on the connector pins. Typical PoE connectors are either made out of plastic or metal and mostly use an unshielded cable. The power lines go through a bridge rectifier and an isolated converter. The MOSFETs of bridge rectifier are very susceptible to ESD on the pins.
- Fails in application when qualifying system level ESD, production yield loss at application manufacturer, TLU leading to damage.
- Customer just says they are field failures. Sometimes we get parts back to do FA and sometimes we do not.
- ESD voltage higher than spec at specific pins
- Customer related application test failed with applied System-ESD pulses
- The "real world" failure may be characterized as a customer choice to apply "port" testing to non-port pins. The closest to "port" pins would only be accessible during device repair with the case removed. In these cases, the interface pins to other subsystems are rarely damaged. Pins which are neither ports nor interfaces to other subsystems within an opened chassis may fail contact or air discharge testing.
- IC may not be designed for IEC robustness, but part is used in application subject to IEC robustness requirements. Customer does IEC testing on IC part / part in prototype system and sees the issue
- customer doing ESD system testing following ISO 10605 plus OEM requirements
- Charged devices in pick-and-place, and charged systems being discharged by other-than-humans.
- EOS due to exceeding AMR, (2) fast transient events like PESD, EFT, or CDE causing various hard or soft failures
- discharge to a non-certified Dual SIM extender connected to the SIMcard port
- ESD/EOS events in SMT, FT, qualification, and end-user operation stages
- Customer release test for control element.
- Rarely given sufficient data from customer to replicate. Simply fail in their system, with no meaningful feedback

[Q06] Can you describe the type of failure (thermal, dielectric breakdown,…) and the failure location (TVS diode, on board resistor,, on chip metal, input or output transistor,…)?

- junction/dielectric breakdown, over-current, etc.
- EOS
- On antenna switch (on chip) - thermal, transistor failure. On chip - dielectric breakdown
- dielectric breakdown
- dielectric breakdown, ESD pinhole, chip metal, connector metal, surge. etc.
- One case was thermal failure. one case was dielectric damage.
- The TVS diode still good but amplifiers fail.
- Pin melt
- metal and junctions
- thermal. chip metal.
- dielectric breakdown at antenna input capMIM

- Type of Failure: Melt filament; Failure Location: On-chip transistor
- dielectric breakdown - Capacitor
- Thermal damages in on-chip IEC protection.
- Because of RF application, TVSs are too capacitive. Because of cost, customers also do not like placing shunt inductors on the board. Typical failure is to an IC connected to the antenna port.
- on chip circuitry and on chip ESD protection
- thermal destruction of silicon
- Physical destruction of IC pin (only local pins) but the housing of the product got destroyed during lifetime (due to weak construction) and hence ESD could enter the PCB. After housing re-design no more failures occured.
- Thermal, IC internal protections. 2) TVS Diodes
- Overstress failure of MOSFET. Typically gate oxide damage.
- Thermal and dielectric breakdown in IC at IO and in internal circuitry
- I usually do not get this type of information. A portion of the failures are usually EOS.
- thermal damage, @on-chip metal
- Na
- Depending on network, slow 330pF/2kOhm pulse showed damaged resistor and fast 150pF/330Ohm pulse showed damaged ESD protection on board.
- Common failures are thermal damage from testing or pin-hole gate damage from assembly floor. Damage is on-chip, most commonly at ESD diodes or I/O transistors
- Physical thermal / electrical damage from overcurrent, often extending well beyond pin to IC metal / internal circuitry.
- I have seen both thermal and dielectric breakdown on chip, at ESD protection or IO circuitry.
- thermal failure (fillamentation) in on-chip ESD protection, dielectric breakdown in functional circuitry
- Primarily energy (therm) and current (fusing) in most digital I/Os. Soft errors #2. Distant #3 Dielectric in RF inputs.
- (1) Damage due to burning out ESD diodes or ESD clamps or due to snapback damage to IO drivers, (2) Latchup in the IO pad, the chip core, or an analog IP block, (3) soft failures like resets or code glitches
- thermal of on chip ESD or internal circuit
- thermal, on chip large melting area of metal and silicon of the output transistor and ESD protect
- usually breakdown on input/output transistors or protection circuits.
- Failures vary, but usually result in system malfunction.
- Flashover from control element to control unit cable, then triggering of the central ESD protection of the IC in the control unit. As the central ESD protection was designed for passive ESD, this led to damage in the IC.
- Full spectrum of TVS diode/board level component/IC on-chip and both thermal and E-field driven fails

[Q12] What else do you follow for your setup?

- contact mode
- For air gap we use a controlled movement of the gun and special fixture for DUT
- ISO10605 test setup with ground plane or with field coupling plane.

- Do you use an IEC61000-4-2 table set up (including standard coupling planes, grounding scheme, etc.) + Robotic system
- HMM/ISO10605 - like set-up (direct grounding)
- Na
- IEC62228-3
- Primary focus on characterizing end-user environment, not qualification to standard.

[Q14] Breakout boards - can you please describe?

- Evaluation boards are used to power up the part for the test. ESD generator is then connected directly to antenna port connector
- Short Cable connection and reconnection
- interface board
- Special designed board to allow contact and air gap injection into DUT
- Only lead PIN outside
- ESD of production line
- short cable adapter
- PCB with minimum set of external components. PCB is NOT comparable with customer application.
- We use special PCBs for a robotic setup, these PCBs are far away from any real application
- HDMI breakout board with exposed wires/test points to discharge ESD gun/TLP
- Provide by product engineer
- Small PCB or application PCB with discharge points
- We use a pogo pin that the gun tip can reliably sit on.
- IC has extender pin cables to allow direct cable pin injection
- Pragma "ZAPADAPT" Coax-to-USBIOs, etc.
- breakout boards with connector to the system port and a fan out of the signal lines to metallic test points for the IEC 61000-4-2 Gun discharge
- breakout bards to access IC package pins; breakout boards to connect pulse generator to a system
- Either a pin extension or an entire test board due to field coupling investigations
- As defined in SAE 2962 and IEC 62228 as well as internally developed solutions

[Q15] Breakout cables - can you please describe?

- Cabling only used to connect power and control pins
- communication cables and such as coaxial
- interface wires
- short stubs with balls to minimize arcing
- Only lead PIN outside
- ESD of production line
- mating connector with very short wires
- sometimes a short cable harness is needed for e.g. satellite sensors and the pulse is applied directly on the cables
- Cable with exposed center cable

- none
- May be wires or coaxial cable
- Entry point with split coax injection.
- no
- small 10mm pin extension
- As defined in J2962, IEC 62228 and custom applications

Note:
- *SAE 2962: CAN transceiver ESD testing*
- *IEC 62228-6:2022 specifies test and measurement methods for EMC evaluation of peripheral sensor interface 5 (PSI5) transceiver integrated circuits (ICs) under network condition*

[Q24] What are the field scenarios for which you observed correlations?

- hot plug, cable discharge, supply overshoot..
- Failure symptoms and reproductive
- I would say that I don't understand well.
- less robustness - more feedback
- 60% mechanical damage also
- We pass internally and don't see failures in the field.
- maybe cable discharge
- USB/Antenna
- Production plant, after sales repair and customer's operation.
- Where customer already identified failures from IEC tests.
- Ungrounded humans before entry into EPA
- Typically, all we are told about the returned part is that the mobile device can no longer communicate. Most of the time, I can reproduce the damage found by discharge into the antenna port.
- More returns are onbserved when no external protection is used i.e. TVS
- Integration challenges: poor grounding, absence of or misplaced TVS, CDM/CBE, instances where large currents can mesh through parallel paths into a DUT
- Systems that had high field returns for known ESD issues tested at low ESD robustness in lab
- low-cost systems w/o dedicated board level ESD protection devices
- direct wiring out of IC pins to exposed parts of the system
- human-being and environment induced ESD event

[29] Can you provide details on the higher target levels for the IC interface?

- none
- From bump/pad, not only ESD cell design but also core devices and some extra components need to be considered
- 8kV
- Should protect 4KV
- to more is integrated (at high silicon cost) the more easy and compact integration will be possible
- 8kV
- LIN, PSI5

- We want to see >30A 100ns TLP for IEC pins.
- 4kV
- USB
- Customer requirement
- 15kV contact 25kV air
- 15kV 61000-4-2 15kV ISO10605
- NA
- not applicable, design is done for system ESD pulse. No direct correlation from increased HBM/CDM levels to higher system ESD robustness (much stronger depending on PCB components, PCB layout, test setup, etc.).
- Normally, the combo (IC/TVS) with better performance and within a budget is chosen, so target levels not always the same.
- (VF-)TLP-HMM correlation + SEED
- Only that customers either want headroom and ask to pass 10kV IEC, or they ask to test up to failure, so they know what kind of headroom there is above 8kV IEC.
- Customer requirements due to application driven ESD risk
- ????
- Higher target levels are driven by competition
- Goldilocks. "Too weak" and it cannot be protected. "Too strong" and the system protection cannot trigger.
- Design the ESD protection using a PESD current waveform as the stress source
- LIN, PSI5
- minimum current target of 2A @50ns
- Difficult, as the IC design together with the external circuitry results in robustness...it is important to find the cost optimum

[Q32] Any other comment you want to add?

- NA
- We do see some correlation between the results of IEC61000-4-2 testing of antenna pins and the results of the same test on the antenna port in the mobile phone but not always.
- SL-DPE is a kind of overload on IC ESD design.
- In my opinion, 61000-4-2 should be a system chassis test, not targeting internal port discharges
- None
- on-chip ESD measures are expensive, SEED needs to be optimized
- None
- no
- n/a
- Answer to Q19 assumes no access to an actual IEC 61000-4-2 tester.
- Questions partly unspecific e.g. what do you understand under real world in question 2. There is no real correlation between IC robustness and systemlevel robustness.
- Many questions are no clear enough (e.g. what are "real world failures"? is it at end customer side or everything after IC is sold? A general comment to the topic: For the additional SL-DPE I see a lot of efforts coming for IC supplier, on the other hand I cannot see a) a correlation from SL-DPE to real system robustness and b) an improved system robustness with high SL-DPE. Maybe

you can even have a false security if the IC has a high SL-DPE robustness (e.g. 8kV direct discharge with GND connect) and the system design is done in a way that destruction occurs already at 5kV (and higher levels) on the PCB (similar setup only adding two passive components on PCB).

- Replication of failure mode is often established well, but correlation between failure ppm and DPE levels is missing because of insufficient data
- We recently are being asked to stress the antenna with a total of 420 IEC stresses to the antenna. This is coming from some verbiage in the industry council (paper 3 part 3 on page 109) that over a 100 stresses are needed to catch certain conditions of the system. This is impossible to pass on Front End Modules for mobile. Also, we have very little information on if IEC ratings are reducing field failures. We don't get that feedback from our customers. We suspect there is no correlation but have no data to show.
- Na
- Many customers have differing requirements regarding how tests are conducted and criteria for success. Some designs which are built explicitly to tolerate direct pin injection are harder against such events. For small devices, few customers are willing to pay for the additional silicon area to support higher performance ESD mitigations. Solutions are a function of what can be achieved on-chip economically and what is implemented at system level to address (a) the ESD qualification tests and (b) end-product real world needs (which may not be directly related to one another). I am fearful that this study will encourage more integrators to perform direct pin injection, including subsystem (product internal) interface pins and even purely internal pins. (1) While I see merits to having a more repeatable process for externally facing interface pins, this may encourage a push for the testing of subsystem-internal and then all pins (2) First I would like to see such a progression explicitly deprecated (3) When the above fails, hopefully enough time will have been elapsed such that an internal system test process could be devised. Such a process would include a step-by-step process for conducting the test including aspects such as: (3a) the limits to which EMI shielding are included (3b) equipment calibration/normalization (another ongoing study through the council) (3c) the process for the benign searching for floating conductors before starting testing (3d) emphasis on disspation of affected nets which may not be dissipated through the gun (3e) :
- The IEC needs to allow improvements in IEC 61000-4-2 waveform criteria (minimizing waveform variation, improving criteria for characterization) to improve the wide disparity of waveform results between IEC guns. Much good research is being done and the IEC is ignoring this. Rather than just blanket requirements for IC robustness of system level ESD, customers need education on pitfalls of IC vs. system level testing.
- ASIC vendors treat robustness data required to optimize in SEED as proprietary IP making it difficult to actually design for robustness.
- no
- There is too little structure in test-setup environment to produce meaningful results from this test. Any new standard/best practice/method that is developed will produce more trouble/headache if it doesn't address/specify the exact board/environment the IC is placed in.