

# Industry Council Survey on Latch-up

## Introduction

For the past three decades, the JESD78 test standard and related test standards (JESD17, EIAJ ED-4701/306, AEC-Q100-004) have been employed to ensure a safe level of latch-up robustness for semiconductor components prior to large-scale production and subsequent field use. Consequently, JESD78 has been widely accepted as a standard qualification test. For various reasons including technology scaling, increasing amounts of integration, and the complexity and variety of semiconductor components, the standard has faced challenges addressing the needs of the increasingly diverse semiconductor product space. These challenges have prompted the Industry Council on ESD Target Levels, working with the JESD78 Working Group, to investigate the latch-up standard in today's context and ask fundamental questions like: How is the test standard interpreted and executed across the industry? What real life stress events does the test standard consider? Are the recommended qualification levels appropriate? Do we have evidence that the test method is a good predictor of robustness against latch-up in the field? What changes should be made to the standard to better suit the reality of present day and future products? To this end, an **online survey** was prepared by experts in the industry to help answer these questions. The survey is intended for all individuals in the industry who have some stake in the JESD78 standard including reliability, design, technology, product management, system design, EDA tools, and OEMs. As with any survey, the relevance of the survey results improves with the number of participants, so it is very important to maximize participation. Concerns for confidentiality should not be a barrier for completing the survey as it is **completely anonymous and untraceable** unless the respondent leaves contact information. Respondents that choose to leave a contact email in the survey will receive a copy of the final report from the survey.

## Instructions

The survey can be completed by individuals or groups, although to maximize the number of responses, individual participants are preferred. Depending on your role (for example, a test lab), you might have a different list of questions than an individual with a different role (for example, a designer).

The total number of questions ranges between 60 and 100 depending on your role and answers. The survey is divided in 9 sections. Nearly all questions are optional, so partially completed surveys are acceptable. If a question is not applicable or you cannot answer it, it can simply be skipped.

It is estimated that the survey will take approximately 1 hour to complete. The deadline for completion is September 1, 2020.

Radio buttons (for 'choose only one' questions) are indicated by

Multiple choice (for 'select all applicable' questions) are indicated by

All questions are numbered sequentially. Mandatory questions are indicated by a \*. Most questions are optional. Please skip questions if you do not want to answer or if they are not applicable to you.

Some questions are only applicable depending on the previous answer. That is typically indicated by starting the question like: If yes, ....

## Important notes

Due to limitations of the forms tool, the survey cannot be printed or interrupted and saved for completion at a later time. Therefore, it is recommended to print the pdf version and use that to collect your answers. This also allows discussion with your colleagues.

Once you have answers to all questions that you want to address, you open the **on-line survey** and complete the form. Each question starts with [Qxy] indicating the consecutive sequence number in the pdf text. Depending on your answer the actual question number in the survey may differ.

Alternatively, you can start the on-line survey and leave it active indefinitely without logging out.

While taking the on-line survey, it is possible to go back to previous questions, but there is no 'undo' function.

## Links

The online version is available [this link](#):

<https://forms.office.com/Pages/ResponsePage.aspx?id=06FuaCu8b0ypLNmcXDAWNd4mfOjifjpOvTIBugeyXKFUMTFCSDQzN1hXRZHVfJHUIAwSDAwQU5MVy4u>

or via this QR code:



## 1. Affiliation and Background

*This section collects some general background information of the respondent*

1. Which company do you represent? (open question)

2. In which country are you working? (open question)

3. Which market segments does your company serve? \*

- Aerospace
- Automotive
- Consumer
- Industrial
- Medical
- Military
- Other (please specify)

4. What type of business is your company? \*

- Fabless IC Supplier
- Foundry
- IC Supplier with Fab
- IP Provider
- OEM
- Test House or Equipment Maker
- Tier/subsystem
- Other (please specify)

5. Which IC product types do you support?

- Very low voltage IC ( $\leq 2V$ )
- Low voltage IC ( $>2$  and  $\leq 5V$ )
- Medium voltage IC ( $>5$  and  $\leq 12V$ )
- High voltage IC ( $>12V$ )
- Analog IC
- Memory IC
- Mixed signal IC
- Power IC
- RFID/RFIC
- Other (please specify)

6. How many latch-up related customer complaints does your company receive per year (approximate number)?

- None

- ≤ 5
- 6 to 20
- 21 to 50
- 51 to 100
- > 100

7. Are you filling out the survey for the whole company or just a part of it? \*

- Whole company
- Business unit
- Product line
- Department
- Group
- Individual

8. Which aspects of the JESD78 test standard are you familiar with?

- Pass/Fail criteria
- Immunity levels classification
- Detailed test procedure
- Special pins
- Reporting requirements
- Maximum stress voltage (MSV)

9. Do you think that the JESD78 standard is useful to prevent system failure caused by over-current or over-voltage in real world scenarios?

- Yes, all cases
- Yes, some cases (please provide examples)
- No

10. Please provide examples of the above reply (open text)

11. Have you experienced latch-up failures?

- Yes
- No

12. If yes, where have you experienced latch-up failures?

- JESD78 testing
- Inline screening test (e.g. Burn-in)

- Reliability testing other than JESD78 (e.g. HTOL)
- Functional test at package-level
- Functional test at probe level
- System level testing (e.g. IEC 61000-4-x)
- Field return
- Other (please specify)

## 2. Case Studies and Field Returns

*This section focuses on the occurrence rate and conditions of latch-up failures*

13. Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?

- Yes, for both I-test and Overvoltage test
- Yes, only for I-test
- Yes, only for Overvoltage test
- No

14. If yes, were the actual stress levels reported to the customer?

- Yes
- No

15. If yes, did that part have any latch-up related field returns?

- Yes (please specify approximate return rate)
- No
- Too soon to tell (recent qualification)

16. If yes, please specify approximate return rate (open text)

17. If yes, were there any measures taken at the board/system level to mitigate the latch-up risk (e.g. add board-resistor, etc.)?

- Yes (please describe)
- No

18. If yes, please describe measures taken (open text)

19. For products that have had latch-up failures in the system, what were the operating conditions needed to replicate the failure?

- Within maximum operating conditions per datasheet specification
- Outside maximum operating conditions, but within absolute maximum ratings (AMR) per datasheet specification
- Outside absolute maximum ratings (AMR) per datasheet specification
- With System level stress testing (e.g. IEC 61000-4-x)
- Other (please specify)

20. For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?

- Due to IC design issues (e.g. poor layout), design not fully compliant with latch-up design rules
- Due to IC design issues (e.g. poor layout), design compliant with latch-up design rules
- Due to a weak board design
- Due to the JESD78 test method not sufficiently covering the applied stress type in the system (e.g. transient stress)
- Due to the JESD78 test levels (+/-100mA or 1.5 x Vddmax) not sufficiently covering the applied levels in the system
- Other (please specify)

21. What percentage of your company's product respins were due to latch-up failures in a system application?

- None
- ≤0.1%
- >0.1% and ≤1%
- >1% and ≤5%
- >5% and ≤10%
- >10% and ≤50%
- >50%

22. Has your company experienced latch-up EIPD (Electrical Induced Physical Damage) with parts that passed JESD78 testing at the semiconductor supplier?

- Yes
- No

### 3. Goal and Testing Strategy

*This section focuses on how and why latch-up testing is done*

23. Is JESD78 testing a product qualification requirement in your company?

- Yes, all products
- Yes, only for certain product types (please specify which)

- No
- No, we do JESD78 testing only as characterization

24. If only for certain product types, please specify (open text)

25. What is the JESD78 test requirement in your company for products that are offered in multiple packages that use the same die?

- Test all packages
- Test a representative non-production package
- QBS (qualification by similarity) of the worst-case package (from a pin count and/or temperature perspective)
- Other (please specify)

26. What is the JESD78 test requirement in your company for Multi-Chip Products?

- QBS (qualification by similarity) of Multi-Chip Modules with individually qualified dies
- QBS (qualification by similarity) of the worst-case Multi-Chip Module (i.e. embedding all dies)
- Same qualification procedure as a Single-Chip Module
- Other (please specify)

27. What percentage of your company's product has experienced latch-up failures (either in JESD78 qualification testing or in the field)?

- None
- $\leq 0.1\%$
- $> 0.1\%$  and  $\leq 1\%$
- $> 1\%$  and  $\leq 5\%$
- $> 5\%$  and  $\leq 10\%$
- $> 10\%$  and  $\leq 50\%$
- $> 50\%$

28. What percentage of your company's product respins were due to failures during JESD78 qualification test?

- None
- $\leq 0.1\%$
- $> 0.1\%$  and  $\leq 1\%$
- $> 1\%$  and  $\leq 5\%$
- $> 5\%$  and  $\leq 10\%$
- $> 10\%$  and  $\leq 50\%$

- >50%

29. What percentage of your company's product respins were due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?

- None
- ≤0.1%
- >0.1% and ≤1%
- >1% and ≤5%
- >5% and ≤10%
- >10% and ≤50%
- >50%

30. What is the goal of the supplt overvoltage test and IO (signal pin) injection test in the present JESD78 standard?

- Robustness against millisecond time range disturbances
- Robustness against nanosecond to microsecond time range disturbances
- Robustness against generic external disturbances (voltage-driven/low-impedance source or current-driven/high-impedance source)
- Robustness against system-internal disturbances (e.g. transmission line reflections, inductive overshoots, etc.)
- Other (please specify)

31. Does the JESD78 testing address real world stress events like HBM and CDM do?

- Yes
- No

32. If JESD78 testing were removed as a qualification requirement for the industry, what would happen?

- Components would be less reliable in the field (please specify why)
- It would have no effect (please specify why)

33. Please specify why (open text)

34. Do you require detailed JESD78 information from an IC Supplier?

- Yes, detailed information is needed
- No, JESD78 compliance is just a check box item



35. Do you scrutinize the JESD78 information provided by an IC Supplier?

- Review of the datasheet or qualification report
- Require a minimum robustness level for all pins
- Review of the vendor's JESD78 test program and pin-by-pin results
- Focused test review on high risk pins in the system
- Yes and we repeat JESD78 testing on supplied parts
- Other (please specify)

36. How are JESD78 test results provided in an IC Supplier datasheet or qualification report used for system design?

- Limit the on-board currents
- Limit the on-board overshoots
- Limit both the on-board currents and overshoots
- Not used
- Other (please specify)

37. Would increasing the overvoltage or injection current levels of JESD78 decrease the latch-up failures in the field?

- Yes
- No

38. Is the operational state of an IC used during JESD78 testing (i.e. low power mode, stable current) representative of real-world applications?

- Yes
- No (please specify why)

39. If not, please specify why not (open text)

40. If a product has multiple modes of operation, how does your company test for JESD78 latch-up?

- In all pin functional modes (e.g. digital and analog on the same IO)
- In all IC functional modes (e.g. full power, partial power down, etc.)
- In permanent reset mode
- In default IC and pin functional mode after reset/power up
- Other (please specify)

41. Does passing JESD78 testing guarantee latch-up robustness in the field?

- Yes
- No

42. If no, what other tests should complement the JESD78 testing to guarantee latch-up robustness in the field?

- Cable discharge
- Single event latch-up (SEL)
- System level stress
- Transient latch-up (CDM/System level time scale)
- Inductive load switching
- Power-up conditions/ground reference differences
- Other (please specify)

#### 4. Next steps of Latch-up testing

*This section collects inputs for possible new directions of latch-up testing*

43. What other types of latch-up tests does your company perform to qualify a product?

- Cable discharge
- Single event latch-up (SEL)
- System level stress
- Transient latch-up (CDM/System level time scale)
- Inductive load switching
- Power-up conditions/ground reference differences
- Other (please specify)

44. If new latch-up testing methods were to be developed in the future what would be your preference? \*

- Keep present JESD78, nothing else needed
- Keep present JESD78 and add new standard(s) covering the above selected events
- Keep present JESD78 and include new settings/tests covering the above selected events
- Replace present JESD78 by a new test method(s) covering the above selected events
- Other (please specify)

45. Often, power supplies in applications are not capable of sinking current and can only source current. Such supplies would limit positive injection current into the IO pin in the application. Should the standard take into account the ability of a supply to sink current when defining current injection level for qualification?

- Yes
- No

46. If a JESD78 stress condition results in a sustained decreased current, should it be considered as a JESD78 failure reason?

- Yes
- No

47. Which of the following circuit elements, if turning on and causing the sustained increased current, should be considered JESD78 failure reasons?

- Parasitic thyristor
- Designed thyristor (SCR)
- Bipolar (parasitic or designed)
- Latching BigFET trigger circuit
- Other latching circuitry (please specify)
- Anything that causes increased supply current

48. If you selected 'Other latching circuitry', please give examples of latching circuits that should be considered a failure in the above situation (open text)

49. Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?

- Yes
- No

50. Which conditions should be included in this new test method(s)?

- Sustained high current states
- System resets
- Temperature (room/hot/cold)
- Process corners
- Other (please specify)

51. As the supply voltage of ICs keeps shrinking, below about 2V the 100mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Does this lead to latch-up risks in the application?

- Yes (please specify why)
- No
- I was not aware of this

52. If yes, please specify why (open text)

53. At what minimum JESD78 current injection level are your company's products safe for final application?

- $\geq | +/-10\text{mA} |$
- $\geq | +/-50\text{mA} |$
- $\geq | +/-100\text{mA} |$
- $\geq | +/-200\text{mA} |$
- Depending on pin current capability (please specify)
- Depending on pin function (please specify)
- Other (please specify)

54. Please specify the above answer (open text)

55. At what minimum JESD78 over-voltage level are your company's products safe for final application?

- $\geq 1.1 \times V_{\text{ddmax}}$
- $\geq 1.25 \times V_{\text{ddmax}}$
- $\geq 1.5 \times V_{\text{ddmax}}$
- $\geq 1.75 \times V_{\text{ddmax}}$
- Depending on supply voltage capability (please specify)
- Other (please specify)

56. Please specify the above answer (open text)

## 5. Reporting and design rules

*This section explores how latch-up testing results are reported and used*

57. How does your company report latch-up test results to customers?

- Report passing JESD78 in datasheet
- Report passing JESD78 immunity level in datasheet
- Report passing JESD78 in qualification report
- Report passing JESD78 immunity level in qualification report
- Report the achieved injection current and voltage levels for pins or pin groups in the datasheet
- Report the achieved injection current and voltage levels for pins or pin groups in the qualification report
- No JESD78 results reported

Other (please specify)

58. Does the latch-up robustness level given in the datasheet of an IC impact the purchase decision?

- Yes
- No
- Yes, only for certain applications (please specify)

59. If only for certain applications, please specify which type of applications (open text)

60. What is the most common action that your company takes in case of JESD78 failure?

- Fix latch-up issue in design revision
- Derate reported latch-up levels
- Document in application note
- Internal use only
- Derate AMR (absolute maximum ratings) in datasheet
- Establish MSV (maximum stress voltage) below which there are no failures
- Other (please specify)

61. Should latch-up IC design rules be exclusively driven by the JESD78 requirements?

- Yes (with current JESD78 specification)
- Yes (with future improved JESD78 specification)
- No (please explain why)

62. If no, please explain why not (open text)

63. As the supply voltage of ICs keeps shrinking, below about 2V the 100mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Should design rules be relaxed in such scenario?

- Yes (please specify why)
- No (please specify why)
- It depends on the application (please specify)

64. Please specify the above answer (open text)

65. If you pass all latch-up design rules, what does it guarantee?

- Pass JESD78 testing
- No latch-up issues in the system/field
- Other (please specify)

## 6. Test execution details

*This section asks specific questions on how latch-up tests are executed*

66. The JESD78 standard requires the following clamping limit to be applied during overvoltage testing: (a)  $I_{clamp} = 100 \text{ mA} + I_{nom}$  or (b)  $I_{clamp} = 1.5 \times I_{nom}$ , whichever one is higher. Does your company follow this requirement?

- Yes, for all tester supplies
- Yes, but only for supply under test
- No, use higher value (please specify)
- No, use lower value (please specify)

67. Please specify the above answer (open text)

68. At what maximum temperature does your company perform JESD78 testing?

- Maximum ambient operating temperature per datasheet
- Maximum case operating temperature per datasheet
- Maximum junction operating temperature per datasheet
- Room temperature only
- It depends on market segment (please specify)

69. In case of 'it depends', please specify the above answer (open text)

70. Which latch-up standard does your company use? \*

- JESD78E
- Older JESD78 (please specify version)
- AEC Q100-004 (please specify version)
- EIAJ ED-4701/300-2 method 306 (Jeita)
- IEC 60749-29
- Other (please specify)

71. If you selected 'Older JESD78' or 'AEC Q100-004', please specify the above answer (open text)

72. Which pin types should be exempt from JESD78 testing?

- Pins that are only connected to passive RC components (see JESD78E annex A)
- Reset pins
- Probe-only pins (i.e. exposed for engineering/debug purposes only)
- Flash programming pins (i.e. that are unavailable to the end customer)
- Clock pins
- IO Pins that are always connected to a VDD or VSS supply in the system, as required by the datasheet
- Other (please specify)

73. Which pulse duration do you select during JESD78 testing?

- The minimum of the tester (please specify)
- The maximum of the tester (please specify)
- The default value of the tester (please specify)
- Another fixed value (please specify)
- Product/pin specific value (please specify)
- Other (please specify)

74. Please specify the above answer (open text)

75. What information is needed to create a JESD78 compliant stress test program?

- JESD78 standard document
- Product datasheet
- Product application notes
- Product design technology information
- Other (please specify)

76. Do latch-up tester data logs (current and voltage) get reviewed in your company?

- Yes, in all cases to ensure the test program is correct
- Yes, in all cases to ensure the test program is correct and program execution follows the JESD78 standard
- Yes, only when test outcome is a failure (either during stress or post stress functional testing)
- No

77. How do you systematically ensure that JESD78 testing is executed properly?

- Curve trace signal pins to ensure their correct impedance state
- Review tester data log (voltage and current pre-/during-/post- stress)
- Use oscilloscope to monitor voltage and/or current waveforms on representative pins

- Compare vector readback with expected vector stream
- No specific checking performed - just execute test program
- Other (please specify)

78. What do you systematically measure/monitor during JEDEC78 testing?

- Injected current/overvoltage reaches programmed value
- Supply voltage collapse during stress
- Abnormal supply and signal pin current/voltage during stress
- Voltage/current compliance reached
- Post-stress currents decrease
- Other (please specify)

79. How do you measure/monitor the parameters you selected above?

- Data log review
- Oscilloscope
- Other (please specify)

80. How does your company test products with signal pins that are exposed to external energy paths (e.g. USB; HDMI; etc.) or have an inductive load?

- Test at the same level as all the other pins
- Test at fixed levels higher than +/-100mA and 1.5 x Vddmax
- Test at higher level depending on expected current in the application
- Test only with final application board (no JEDEC78 testing done)
- Other (please specify)

81. For low-voltage (LV) signal pins, the applicable voltage clamping limits of JEDEC78, Table 2 may reduce the injected current below the set target level (e.g. +/- 100 mA). With a maximum supply voltage below about 2V, the injected current may even become zero. Do you strictly apply the Table 2 voltage limits?

- Strictly apply Table 2 voltage limits, even if very little current gets injected into the signal pin
- Characterize beyond Table 2 voltage limits until reaching the maximum stress voltage (MSV)
- Characterize beyond Table 2 voltage limits until reaching a pre-defined injection current target (please specify)
- Other (please specify)

82. Please specify the above answer (open text)



83. If you characterize LV pins beyond the voltage limits of JESD78, Table 2, do you apply this extended test method for product qualification and document the extended spec limits in the latch-up report?

- No, do not test LV pins beyond Table 2 limits
- No, the testing beyond spec limits is only done for internal characterization
- Yes, apply extended spec limits, but do not mention them in latch-up report
- Yes, apply extended spec limits and document them in latch-up report
- Other (please specify)

84. Do you setup the JESD78 test program to check if the injected signal pin itself suffered from latch-up ("signal pin latch-up")?

- No, only consider latch-up on power supply pins
- Yes, also check "signal pin latch-up"
- Other (please specify)

## 7. Maximum Stress Voltage (MSV)

*Maximum stress voltage (MSV) is a latch-up specific term. The questions assess how this is perceived and used in practice.*

85. The concept of maximum stress voltage (MSV) allows one to differentiate between latch-up and EOS (electrical overstress). The conventional pin voltage limits during JESD78 testing may be reduced to the MSV. How do you determine the MSV?

- Do not use MSV
- Dedicated MSV test procedure - step up voltage until damage
- Adjust voltage limits during JESD78 testing until it passes
- Use product absolute maximum rating (AMR) values
- Use technology absolute maximum rating (AMR) values (typically provided by fab/foundry)
- Simulations
- Other (please specify)

86. For determining the MSV, do you confirm that the damage is from a stress mechanism not directly related to latch-up (as required by the JESD78 standard)?

- No
- Yes, with physical failure analysis (FA)
- Yes, by other means (please specify)

87. In case of 'other means', please specify the above answer (open text)

88. Which (irreversible) damage conditions do you find acceptable for invoking the MSV?

- Interconnect (metal, bonding, via) failure
- P-N junction breakdown
- Gate oxide rupture
- Bipolar snapback
- Other (please specify)

89. How often do you encounter a product where the MSV reduces the injected current below the set target level (e.g. +/-100mA)?

- Most of the time
- Often
- Sometimes
- Rarely
- Never
- Do not use MSV

90. Do you set the pin stress voltage limits so that they do not exceed the product AMR?

- Yes, if damage occurs while exceeding the AMR, it is not a latch-up failure
- No, the AMR is not applicable to latch-up testing

## 8. Failure criteria

*This section collects questions on determining pass/fail results of JESD78 testing.*

91. If latch-up occurs during the stress pulse (but not sustained), should that be considered a failure?

- Yes
- No
- It depends (please explain)

92. Please specify 'It depends' (open text)

93. What are common causes of rejecting a JESD78 pass/fail result?

- Incorrect specification/request
- Setup instability
- Current or Voltage instability during the stress
- Desired injection levels not reached
- MSV exceeded

- Tester instability
- Latching not due to parasitic thyristor
- Other (please specify)

94. Do you use functional test (ATE test) to verify device specification requirements after latch-up testing to confirm pass/fail result from tester?

- Yes
- Yes, but do not count as failure
- No

## 9. Conclusion

*This is the last section of the survey. Please take some time to consider entering suggestions, feedback, or recommendations. If you leave your email address you will receive a copy of the final report as soon as it is ready.*

95. Feel free to enter any suggestions/recommendations (open text)

96. Please provide your email address to receive a copy of the final report on this survey (open text)