Industry Council Launches Survey on Latch-up

Latch-up, which is the triggering of a low-ohmic path between power supply rails that can either damage the IC or make the IC inoperable, became a reliability concern in the mid 80's. The first practical Industry IC latch-up testing method with injection current requirement, JESD78, was published in the mid 90's by JEDEC and has been revised five times by the JESD78 Working Group (see Figure 1). The IO test method essentially tests latch-up robustness by trying to inject a ±100 mA current with a clamping voltage applied to the pin which could be limited by the maximum stress voltage (see Figure 2).

For various reasons including technology scaling, increasing amounts of integration, and the complexity and variety of semiconductor components, the standard has faced challenges addressing the needs of the increasingly diverse semiconductor product space. Some of those challenges are:

- It is unclear how this test method correlates to real threats.
- In many low-voltage cases, the current injected in the IO is very limited.
- There are many technicalities that can disqualify a result. Examples are the active state of the DUT, the definition of special pins and power supply instability.
- There is confusion about the method and its results. Examples are the required temperature setting, the definition of LDO pins and the use of the maximum stress voltage.

After publishing well received white papers for HBM, CDM, system level ESD and EOS, these challenges have prompted the Industry Council on ESD Target Levels, working with the JESD78 Working Group, to re-evaluate the latch-up standard in today's context. To understand more on how people are dealing with the topic and to get more information on how the Industry uses latch-up testing results and to understand what Industry expects from latch-up testing, the Industry Council has set up a concise, yet detailed, survey.

Questions that can be considered in this light are e.g.:

- How is the test standard interpreted and executed across the industry?
- Which real-life events does JESD78 intend to simulate? Do these occur in present day applications?
- Why does the test specify ±100 mA for IO assessments? Are the recommended qualification levels appropriate?
- The prescribed voltage compliance limits prevent any significant current injection for low voltage pins. Is that intended and/or desired?
- The formal latch-up definition describes parasitic thyristors. Should latch-up testing only be concerned about that? What about latching of other structures under the same conditions?
- Do we have evidence that the test method is a good predictor of robustness against latch-up in the field?
- What changes should be made to the standard to better suit the reality of present day and future products?

The goal of this survey is to provide clarification on the test execution and use of the testing results and to derive recommendations, based on the data collected from a wide audience, for future directions of the JESD78 standard and potentially other standards. The data analysis and the recommendations will be

published in a white paper prepared by the Industry Council on ESD target levels and shared with the JESD78 Working Group.

The survey can be accessed through this link or the QR code below the text. Of course responses will be treated confidentially. The system does not provide options to trace where data comes from, unless the respondent enters contact details. A full pdf version of the survey is also available.

Please forward this message to anyone who may be able to contribute valuable information. All information is welcome and helpful but especially feedback from OEMs and system manufacturers is needed.

More information on the Industry Council on ESD Target Levels can be found here: http://www.esdindustrycouncil.org/ic/en.

Full link to the survey:

https://forms.office.com/Pages/ResponsePage.aspx?id=06FuaCu8b0ypLNmcXDAWNd4mfOjifjpOvTIBugeyXKFUMTFCSDQzN1hXRDZHVFJHUlAwSDAwQU5MVy4u

QR code to the survey:

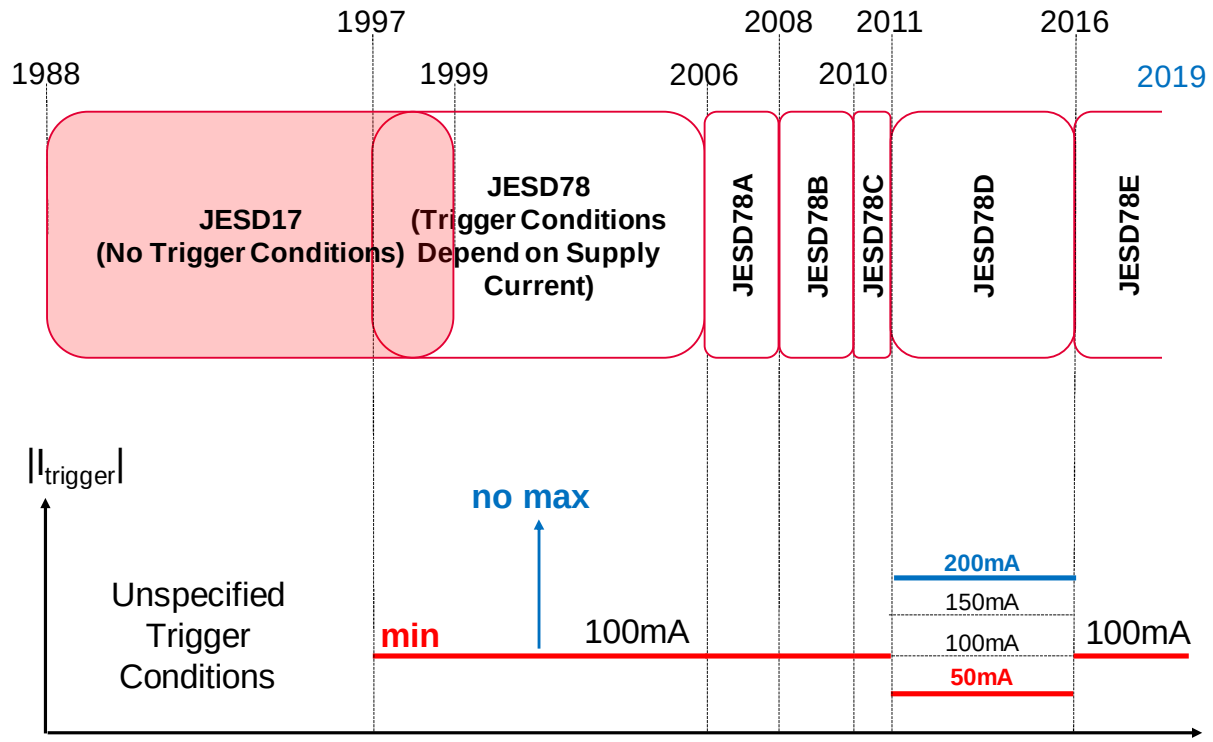

Figure 1: Latch-up Testing Method Revisions and Associated Current Injection Requirements

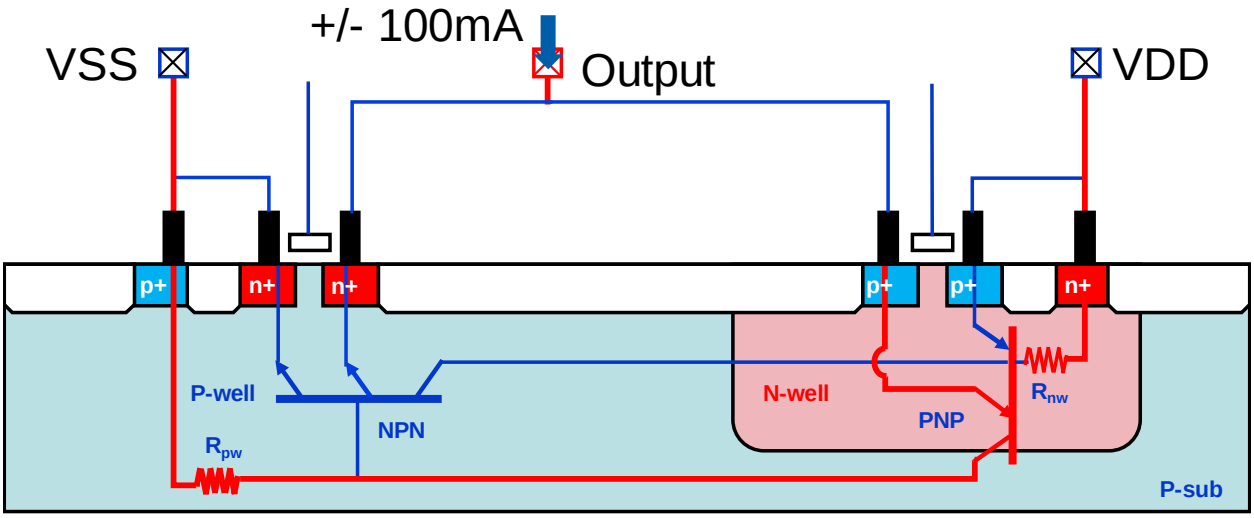

Figure 2: Cross-section of Parasitic Thyristor in CMOS Buffer