Industry Council on ESD Target Levels

MM Qualification Issues

Outline

- Highlight Summary
- Background of the MM Requirement
- Relation of MM to HBM and CDM
- Industry Council Data
- Issues for MM Requirements and Qualification
- Current Positions of Standards Bodies on MM
- Conclusions about MM Requirements
- Customer OEM Positions
- Appendices
  - A: HBM Vs. Failure Modes
  - B: MM Tester Problems
  - C: Industry Council's Data Interpretation
  - D: Interpretation for Automotive Applications

Highlight Summary (1)

- From extensive studies and investigations by leading ESD experts in the industry it can be concluded that:
  - The Machine Model test method specification to qualify ICs does not advance the real world ESD reliability of IC products
  - The MM qualification requirements are unnecessary when both HBM and CDM specifications are both met
- Furthermore, it is also becoming clear that CDM has much more relevance for field ESD reliability, and thus the focus must shift towards the CDM model
- For all future ESD qualification requirements, the Industry Council recommends elimination of the MM qualification
- Well-known industry standards organizations, including JEDEC, the ESDA and JEITA, strongly support this position

Highlight Summary (2)

- **MM testing is redundant to HBM, and does not create relevant ESD failures that differ from HBM**
- **This is true even when one considers the bipolar type pulses that are sometimes reported to be observed in the field**
- **No field failures have been found that would have been prevented by MM testing**
- **Billions of IC components have been safely shipped worldwide using HBM and CDM testing only**

Background to the MM Requirement*

1. Machine Model originated at Hitachi (Renesas Electronics) about 45 years ago and was introduced to Japanese semiconductor customers as a test case to represent the HBM.
2. This test method spread widely to the Japanese customer base, and was later established as an ESD test standard by the EIAJ around 1981.
3. During 1984 someone mistakenly named it “Machine Model.”
4. Then during 1991, the ESDA, JEDEC and IEC adopted this as a new test standard.
5. Later it was realized that the Machine Model name caused a lot of misunderstanding that needed to be cleared up.

*** JEITA Meetings September 2011**

Background of the MM Requirement

- At the time this was happening, there was some confusion between this model and the CDM
- There was also a significant miscorrelation between the MM testers used in Japan versus the testers built in the US/Europe arising from the different test equipment designs

Background to the MM Requirement

- In its early use in specifications, 200V MM had been adopted (without supporting data) to be the safe required level for IC components
- Where did 200V come from? Most (incorrectly) thought that 2kV HBM (I_{p1} = 1.3A) translates to 200V (I_{p1} ~3.5A), and hence the perception for the requirement
- This model and its requirements have spawned much controversy and disagreement amongst various ESD experts throughout the industry

Background to the MM Requirement

- **With advanced semiconductor technologies, combined with the expected higher performance of IC circuits, meeting the old ESD specification levels is rapidly becoming impractical (mostly due to large area protection devices required to meet the associated high current levels)**
- **We present here evidence and arguments as to why the MM qualification requirement is not justified or necessary for safe ESD reliability, no matter what the application may be**

MM Relation to HBM, CDM

- To avoid high charging voltages from the HBM test, MM was thought to be a good substitute with lower pre-charging voltage but with equivalent current stress.
- There was really no intention for MM to address any different failure mechanisms than HBM.
- In the vast majority of cases, analyses comparisons between HBM and MM showed the same damage sites
- This is in contrast to CDM, where the rise time is much faster; often leading to high voltage drops and typically resulting in unique oxide failures

ESD Failures from Manufacturing

- **In the early times, MM was assumed to simulate fast ESD events and would relate to failures from production and assembly**
- **But prevaling data has shown that when ESD field failures (including production / assembly) occur, they are often correlated to weak CDM protection design or poor control of static charging in manufacturing**

Industry Council's Data

- **The Industry Council has done extensive analysis comparing HBM and MM levels on the same devices**
- **These analyses have proved that 2kV HBM and 200V MM are not easily correlated, as was commonly assumed in the past**
- **Based on a vast amount of data collected by numerous suppliers, it was also established that 1kV HBM is more than safe for IC handling and that this level often translates to a minimum of 30V MM**
- **In some rare exceptions it may translate down to <30V, but no data has been found relating this effect to any field returns**

Industry Council's Data

- **Based on the collective knowledge and experience from the Contract Manufacturers represented on the Council, it is well known that with the most basic ESD controls, significant MM events do not ever occur**
- **These studies also established that almost all of the field returns were due to EOS, and very few were related to CDM.**
- **It was further established that low threshold HBM devices produced no more EOS returns than high threshold HBM devices, indicating that the two (HBM and EOS) are unrelated**

Industry Council's Data

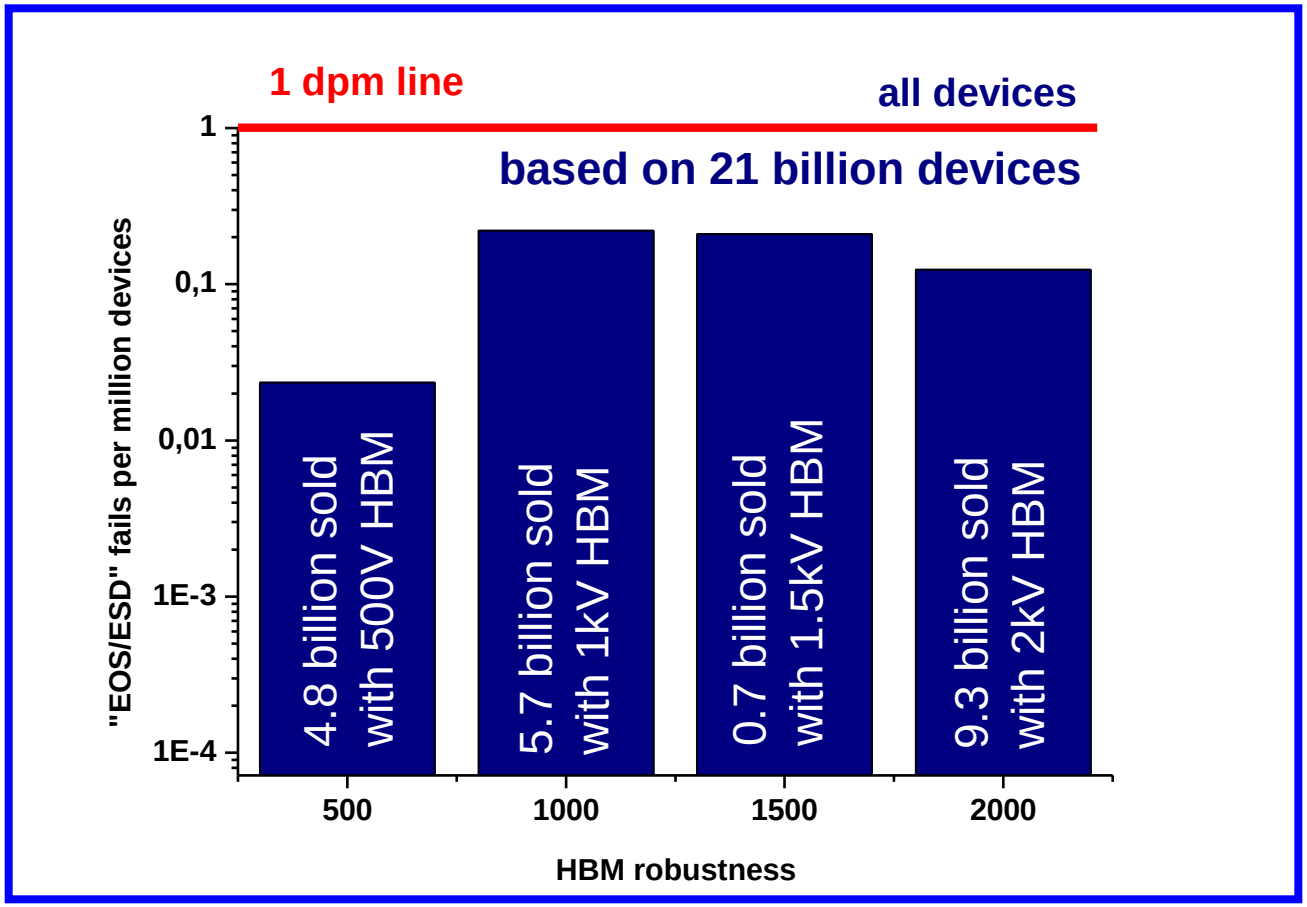
- **As a result, this work has established that:**

  1) If any ESD failures occur, they do not lead to EOS failures as commonly assumed, and

  2) to achieve "zero defects", the true origin of the EOS failures must be understood and addressed rather than relying on artificially high and irrelevant ESD levels (such as 200V MM) as a way of ensuring the overall product reliability

- **All of these studies have been documented and published as a white paper (JEDEC Document: JEP155) in September 2008.**

Field Return Data Tracked With HBM Levels



- Specific product volumes that were shipped at different level of ESD performance
- All products were handled at sites with at least basic ESD control
- Field returns had no correlation to weak pins and failures are only related to EOS
- **Conclusion: 500V HBM products are just as safe as 2kV HBM products**

Indirect Evidence for Field Return Data with MM Levels

- Field data clearly showed that for devices shipped between 500V and 2kV HBM, there is no correlation to the failure return rates (Slide 14)
- *What does this mean for the same devices if they were measured with MM levels?*
- Although this was not exclusively studied, these same units would certainly have different range of values if measured with the MM test
- From the Council's data (see Slides 35 & 36), the ranges would be between 30V and 300V for HBM devices between 500V and 2kV
- Even then, the translated values for MM, albeit arbitrary, would also indicate that the field returns have no correlation to some specific MM level (see Slide 37)
- Therefore one can safely infer that a device's MM robustness has no impact on field return rates

Is MM Really Relevant for Qualification?

- ESD control of machines and fixtures at any manufacturing or assembly site is always critical to prevent potential damage from charged conductors
- Proper grounding requirements are mandatory regardless of the IC's measured MM performance
- While measured MM data is weakly correlated to HBM, in practice any MM qualification data provides redundant and less reliable information

Summary of MM Qualification Issues

- **MM qualification requirements have significant drawbacks including**
  - **No meaning to real world failures**
  - **Redundant if performing HBM plus CDM**
  - **Even if intrinsically related to HBM, the extracted or projected MM test value has no proven relation to metal to metal contact events at production/assembly**
  - **Devices with various measured MM levels have shown no correlation to real world EOS failure returns**

Issues for MM Characterization

- **Even for just evaluation, MM still has several difficult issues**
  - **Any MM test data has no relevance to factory machine control**
  - **Because of the above, the extracted values would not give a robustness comparison of one product versus another**
  - **MM testers continue to have serious reproducibility problems due to parasitic variations, preventing any consistent data correlation from test to test or from product to product**

MM Status

- Customers continue to require the testing although it has been shown that MM testing does not reflect real world component ESD failure modes.
- The Industry Council published WP1 which concluded that while factory machine discharges are real and the control for them is critical at the factory level, the HBM and CDM evaluations sufficiently cover the protection requirements at the IC package level, making the MM requirement redundant.
- However, the MM standard documents available from both JEDEC and ESDA seem to imply to customers that MM test evaluation is critical for device qualification.

➔ Note: Both organizations have been working to clarify this

JEDEC JESD-22-A115C Status

- JEDEC does not recommend characterizing the MM level
- JESD-22-A115C was left on the JEDEC web site to discourage others from pursuing renegade MM test definitions. In general JEDEC does not totally remove any methods, but instead provides use guidance and limitations
- JEDEC has no further interest in redefining, updating or maintaining this model's specifications

JEDEC's New Official Position on MM:

- **JESD22-A115C is a reference document. It is not a requirement per JESD47G.**
- **Machine Model, as described in JESD22-A115C, should not be used as a requirement for IC ESD Qualification.**
- **Only HBM and CDM are the necessary ESD Qualification test methods, as specified in Stress Test Driven Qualification of Integrated Circuits (JESD47G).**

ESD Association Status

- **The ESD Association has decided to downgrade this model to Standard Practice (designation reserved for methods which do not provide repeatable or reliable results)**
- **Neither JEDEC nor the ESD Association recommends doing any MM ESD characterization since the testing consumes considerable ESD / ATE test resources and the results have little relevance.**

Positions of Other Standards Bodies:

- JEITA (Japan) has demoted MM from a standard to a reference method (in 1992), indicating that it is not a qualification requirement
- The AEC Q100 now lists MM only as an option

Outside EPA - Some Important Questions

Will removing MM cause more EOS failures? – **No!**

- Electrical Overstress (EOS) failures occur for different reasons than for ESD
  - Voltage spikes from supplies and misapplications
  - Uncontrolled current events
- Major studies across the industry have found no linkage between the two after tracking millions of products shipped
- No EOS failures related to weak ESD pins
- Field returns tracked with almost all EOS failures are independent of the HBM ESD levels (500V to 2kV HBM) shipped
- The same conclusions apply for these devices shipped without any MM qualification tests

Summary on MM Requirements

- **MM was originally meant to be a worst case HBM method to be tested at lower voltage levels to avoid high voltage discharge equipment.**
- **CDM is a much better representation of machine discharge events, and therefore HBM and CDM constitute the real ESD requirements.**
- **There are no known 100V or 200V MM events in the field. At worst case, machines (that are grounded as required) can acquire potentials in the 15-20V range.**
- **Evaluation with MM does not give any information as to how to address machine ESD control. However, better control of machines in accordance with the S20.20 program is relevant and definitely important.**

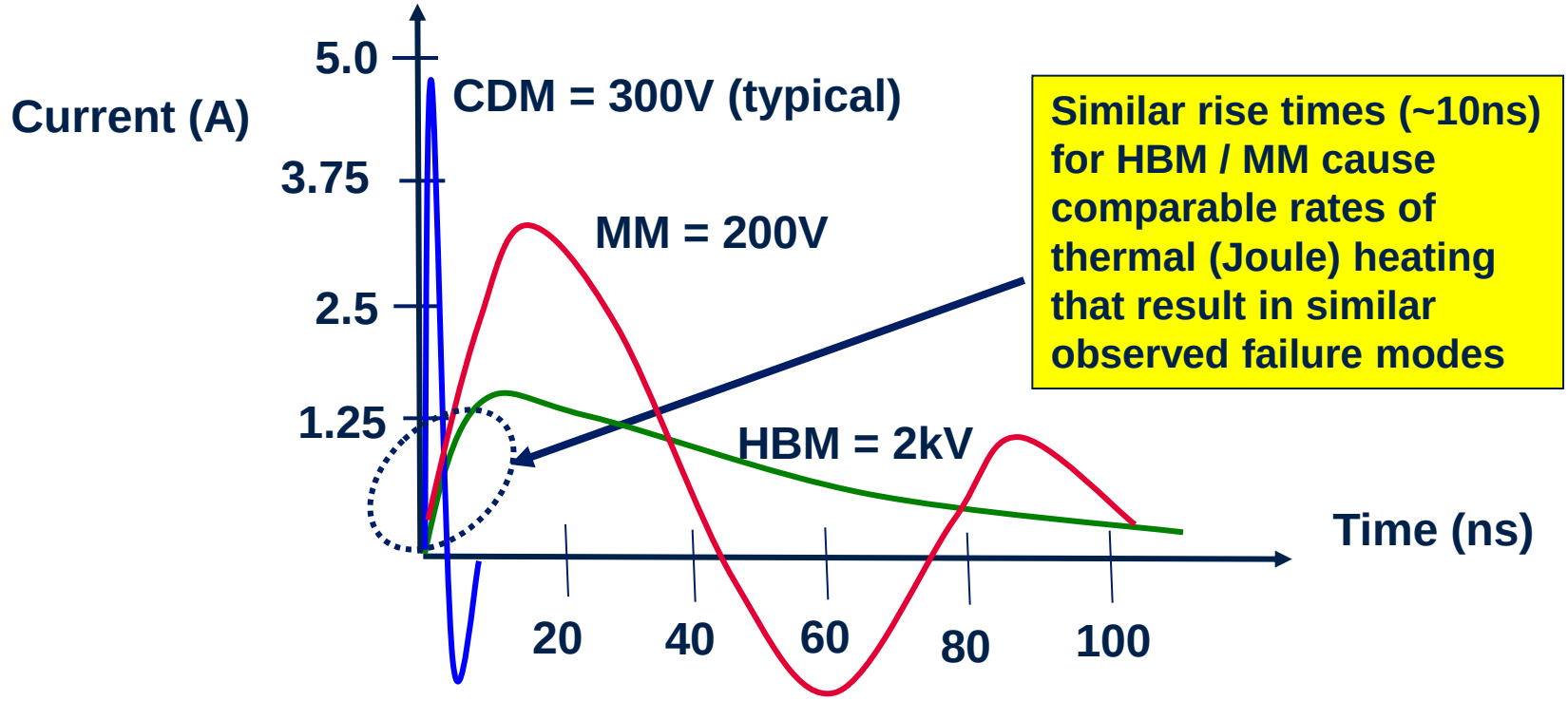
General OEM Positions

- **Several OEMs across the industry have stopped requesting any information about MM**
- **Billions of devices shipped without any MM information (but having met HBM and CDM requirements) show no MM-related failure return issues**
- **Many of these corporations are now confident that this MM information is of no value**
- **Most notably, more companies are now moving to change their qualification requirements by dropping MM altogether**

Appendix A

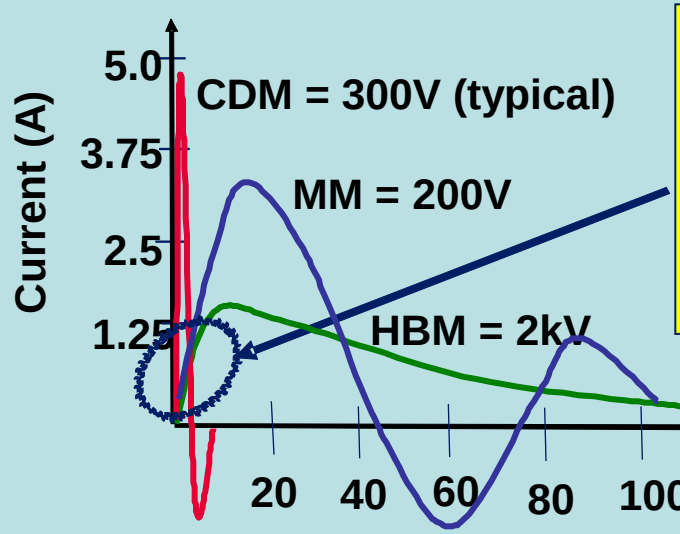
Failure Mode Comparisons Between HBM and MM

Component ESD Waveform Comparison

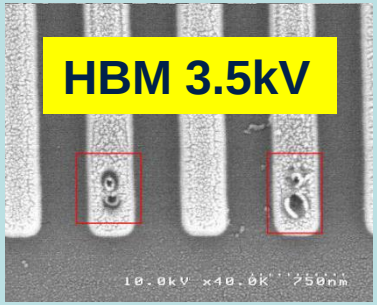


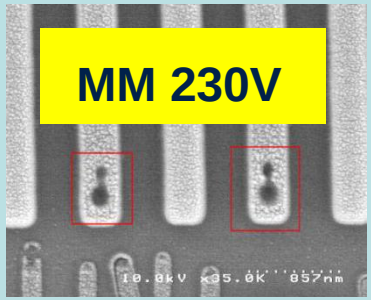
- Due to this thermal effects, HBM and MM give similar fail modes. In contrast, CDM, with its sharp rise time (<0.5ns), gives faster and more severe voltage drops, resulting in unique oxide failures
- HBM and MM failure mode correlations are quite consistent for all advanced silicided diffusion devices
- Even for non-silicided devices, where Joule heating and failure type may be pulse width dependent, historical MM and HBM failure modes have been found to be the same (indicating MM test does not reveal different failure modes)
- Some rare exceptions might result from the bipolar nature of the MM pulse (see Slide 30)

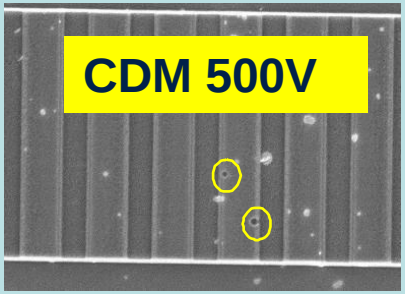
Component ESD Waveform Comparison



Similar rise times (~10ns) for HBM / MM cause comparable rates of thermal (Joule) heating that result in similar observed failure modes; but for CDM the damage is different







- HBM and MM: Same damage in the protection diode of the I/O Pin
- CDM: For the same I/O Pin, the damage is seen in the Output transistor at the Drain-Gate

What About the Bipolar Nature of the MM Pulse?

- There has been some potential concern by a few that MM is bipolar in nature and hence can lead to a unique failure modes.
- Although the MM testers may create this unique failure mode effect in some rare cases, no field failures were ever found which would substantiate this concern
- This again implies that MM test does not address failure mechanisms beyond HBM test with relevance to real world failures

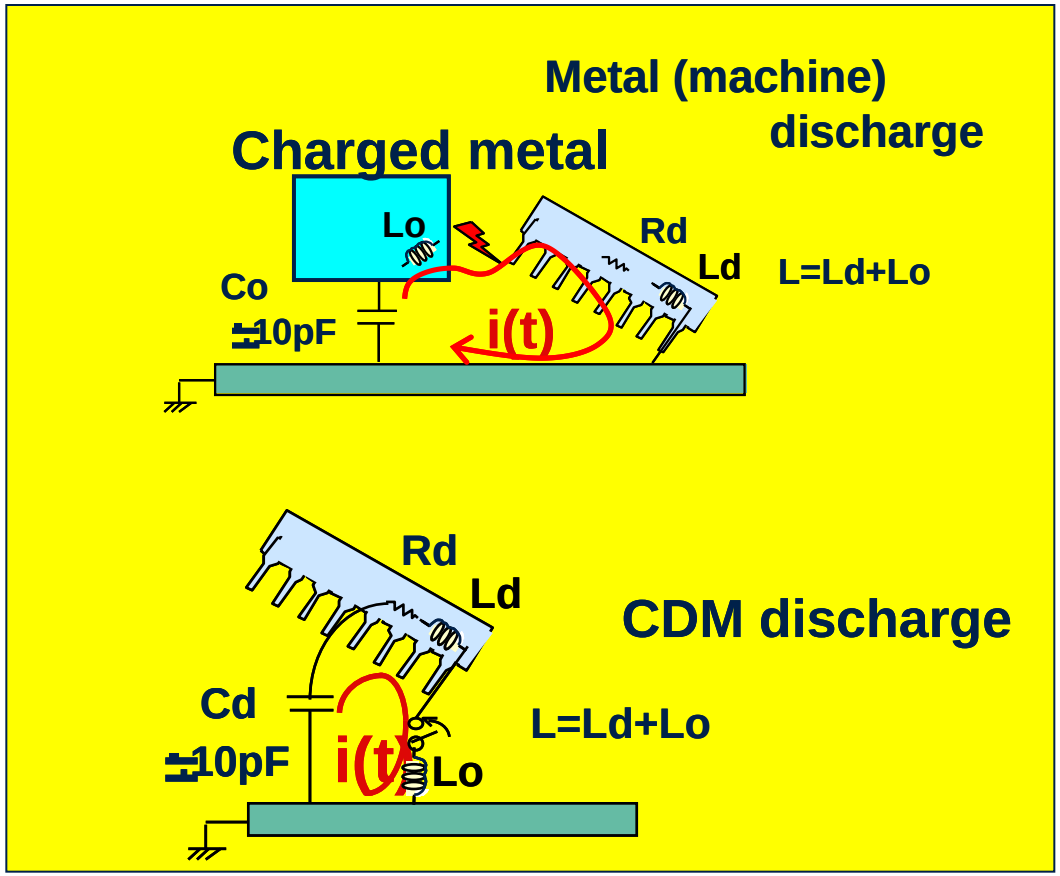
Metal Discharge Versus CDM Discharge

(from the analysis of M. Tanaka et al., ESD Symp. 1994)

This formula can be applied to both cases of the metal discharge and CDM discharge.

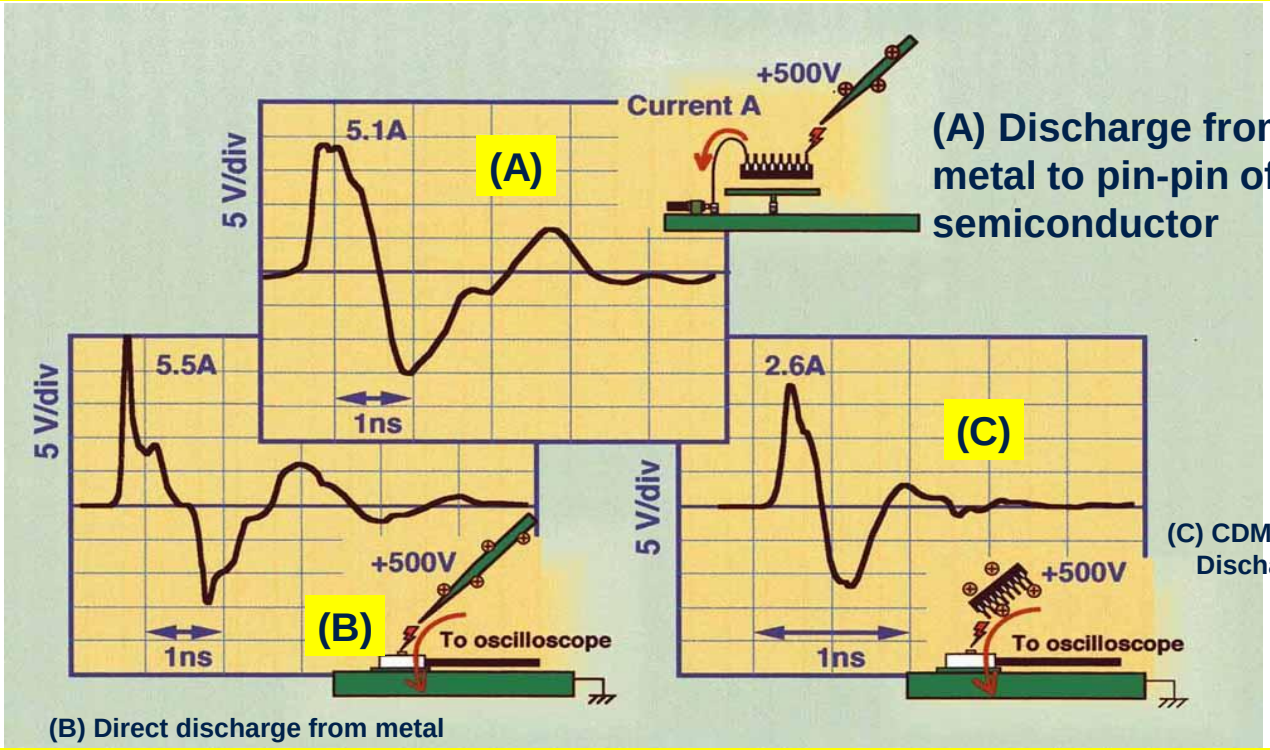
$$i(t) = \frac{V}{\omega L} e^{-\frac{Rd}{2L}t} \sin \omega t$$

$$\omega = 2\pi f = \sqrt{\frac{1}{LCd} - \frac{Rd^2}{4L^2}}$$



Metal Discharge Versus CDM Discharge

(from the analysis of M. Tanaka et al., ESD Symp. 1994)



A: Measured discharge from a charged tweezer to IC pin
B: Measured direct discharge from metal
C: Measured CDM test discharge

➔Metal discharge events are well represented by CDM

Appendix B

MM Tester Issues

Tester Problems

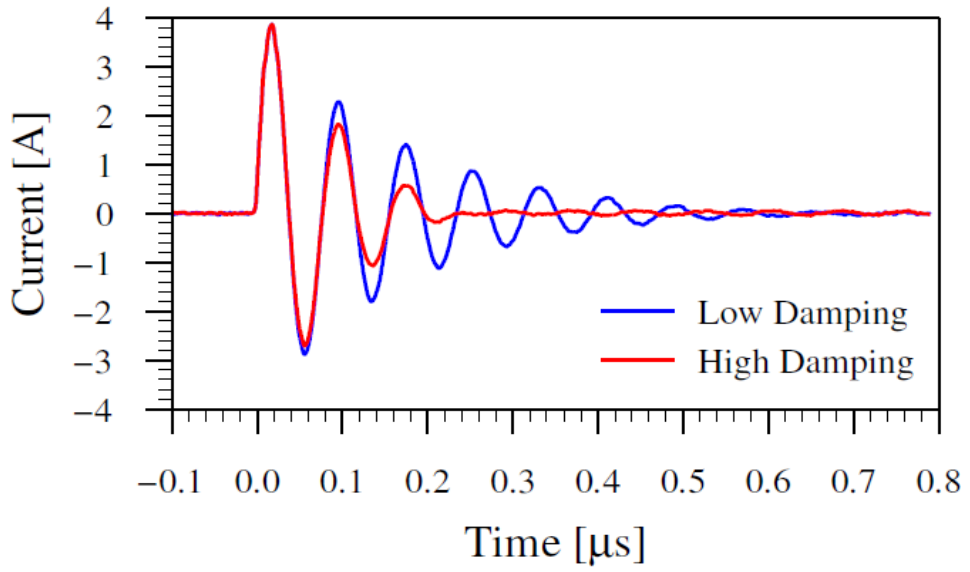
MM: More sensitive to parasitics than HBM

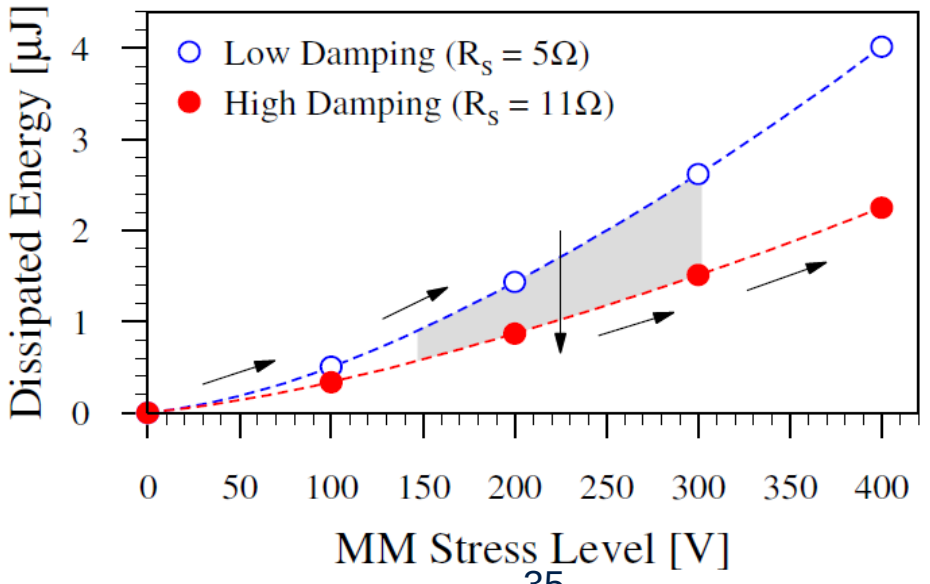
- If parasitics are not controlled, variations between testers will be a problem.
- For MM, the measured protection levels can artificially depend on the location of the pin on the chip.
- Large pin-count device testing will involve higher parasitics and make it difficult to achieve/establish clear MM performance consistently
- It is now being recognized that because of the tester parasitics, the MM measurement is quite an unreliable test

Tester Problems

- One and the same state-of-the-art MM tester can give pulses with different damping for the same stress level.
- The dissipated energy is largely different and the repeatability of MM pulses is poor in the typical test range, especially beyond 100V
- In contrast, HBM is already heavily damped and hence is inherently much less susceptible to parasitics

K.T. Kaschani et al., 13th AEC Reliability Workshop 2008, Novi (USA), 6-8 May 2008

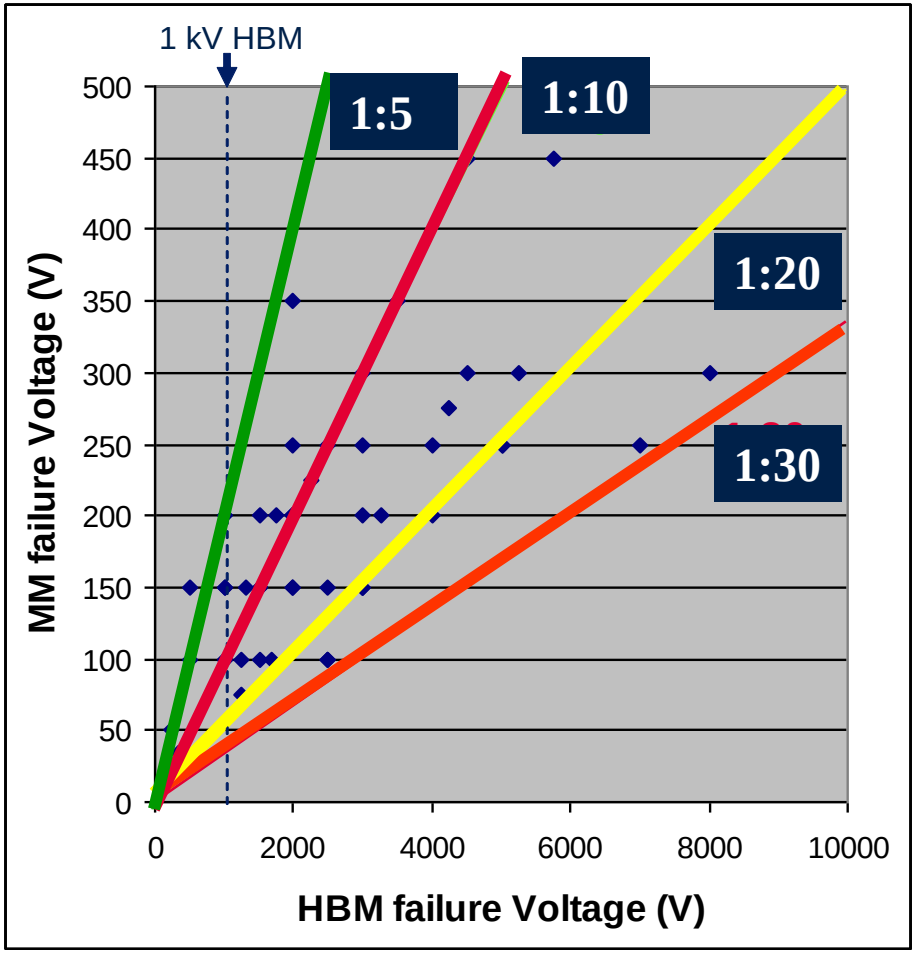




Appendix C

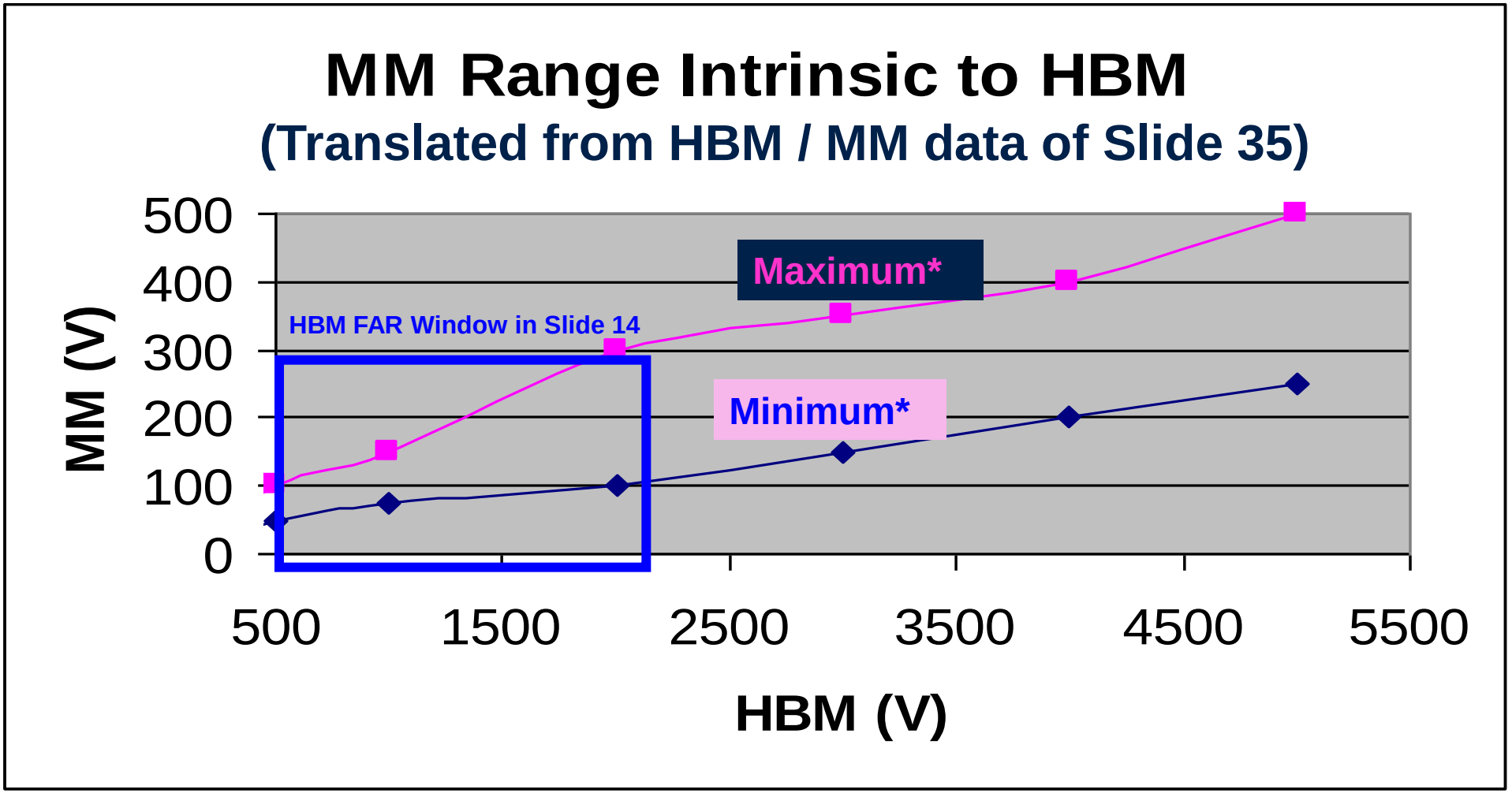
Industry Council's Data and Interpretation

Industry Council's Data: HBM to MM



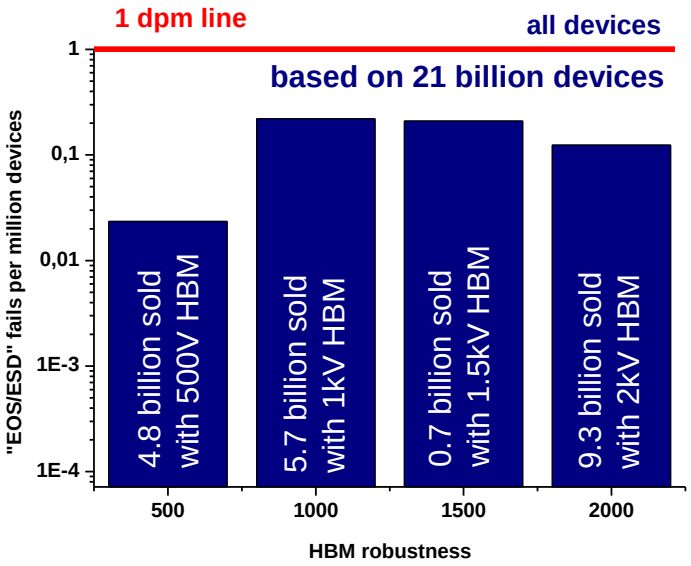
- **When HBM is scaled down, the intrinsic worst case MM level does not reduce at the same rate**
- **All of the data fall below the 1:30 line, indicating that this is a general worst case**
- **But at lower HBM levels, the ratio actually decreases. This reduction at low HBM ranges can come from a combination of lower ESD device resistance effects, voltage drops relating to the MM circuit model, and the parasitics**
- **At 1kV HBM the ratio is 1:10 or lower, and at 500V HBM this moves closer to 1:5**

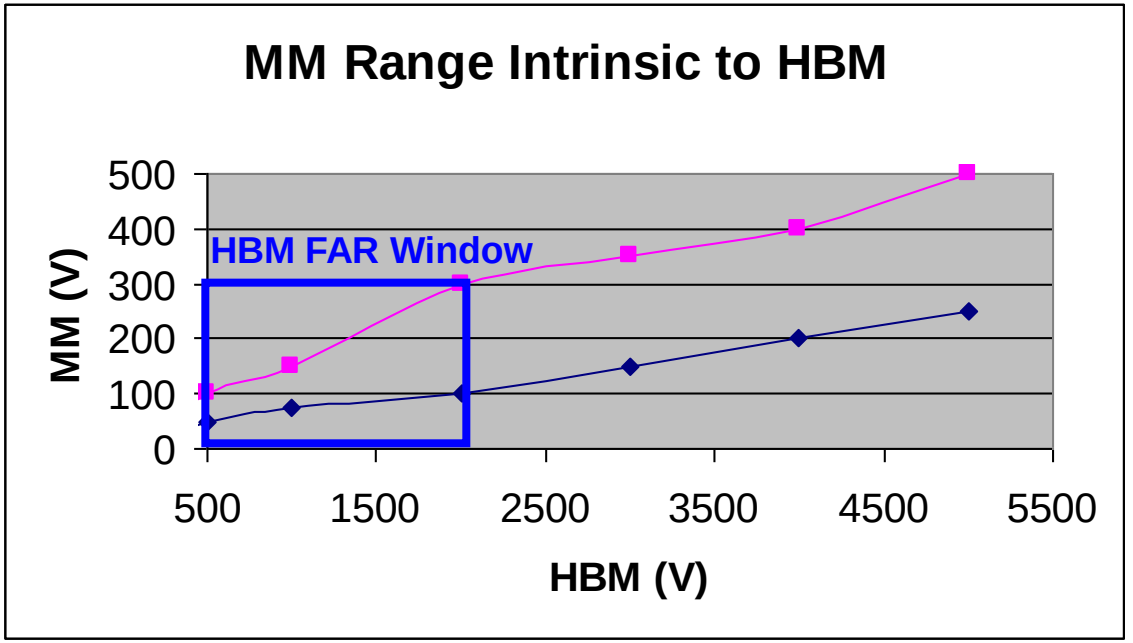
HBM to MM



- Min and Max curves were translated from the data in Slide 37
- The HBM FAR data exists only in the window shown. How can this be translated to MM FAR data?

HBM FAR Window and Translation to MM Field Reliability





- **The HBM units shipped at 500V, 1kV, 1.5kV, and 2kV should have intrinsically translatable MM levels from 50V to 300V**
- **Therefore, the field returns must be independent of 50V MM or 300V MM**

Appendix D

Interpretation for Automotive Applications

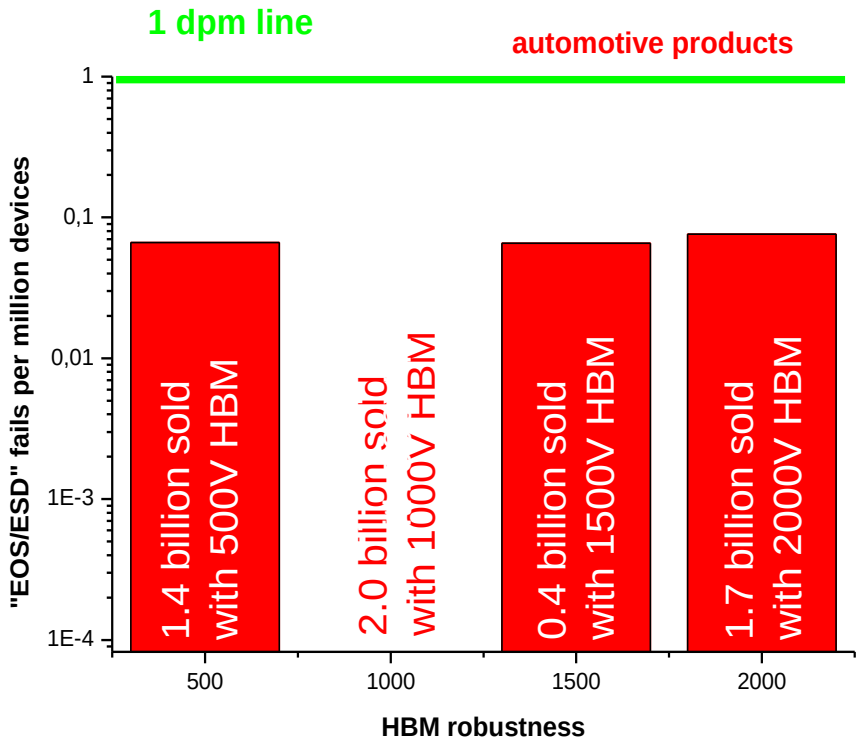
Automotive Dilemma

- The automotive industry pays special attention to knowledge-based specification, design, manufacturing and qualification of ICs
- As a result, there is the demand for ICs to be fit-for-application rather than any consideration of fit-for-standard
- But the MM is not a fit-for-application model as explained in the previous slides
- Thus when the ESD specs are stated (as for MM), the rationale for the requirements needs to be understood
- Therefore we first need to consider if the ESD requirements for the automotive environment are any different from other consumer product environment requirements

Automotive ESD Exposure Scenarios

- Automotive IC supplier use the same assembly sites for IC chip production as the consumer IC suppliers
- However, there exists some inherent concern that automotive ICs must adhere to higher levels of ESD (for production safety and passenger safety) to protect against EOS, than non-automotive ICs
- Additionally, automotive product markets often demand “Zero PPM” for overall IC product reliability that includes ESD
- In actuality, the same HBM non-dependence on failure rate applies to automotive products, as evidenced from product failure returns data (Slide 37)
- This implies that any exclusive MM requirement has no added value for automotive ESD reliability
- An additional, there is concern is that bipolar-like ESD pulses may be more prevalent in automotive systems
- The bipolar issue may be addressed with the requirements for ISO pulse testing on interface pins with the system under application

Industry Council HBM FAR Data – Automotive ICs



- Consolidated data from the Industry Council
- Failure rate phenomenon is independent of the product ESD level
- There were no failures that were seen for the 1kV products
- Any failures instead related to EOS or System Level ESD

Following the same arguments as in Slide 38:

- These automotive IC HBM units shipped at 500V, 1kV, 1.5kV, and 2kV have intrinsically translatable MM levels from 50V to 300V
- Thus the automotive IC field return rates are obviously not related to MM levels

Automotive ESD Exposure Scenarios

Concern: Potentially higher ESD risk in OEM assembly lines since they may have no ESD control in their assembly lines

Reality:

- Only “external” pins are affected (system pins)
- System level robustness is not related to HBM (or MM) ESD robustness
- Automotive OEMs have an obligation to use ESD control in their assembly lines, just as non-automotive OEMs do

Automotive ESD Exposure Scenarios

Concern: Fear of higher ESD risk during repair, since ESD control is low or zero (especially in non-licensed repair stations)

Reality:

- Only “external” pins are affected (system pins)
- System level robustness is not related to HBM (or MM) ESD robustness

Automotive Design Applications

- Many automotive applications including
  - car entertainment
  - automotive networking
  - automotive immobilizers and keyless entry/go
  - etc.
- Many of those are not different from non-automotive, especially with respect to ESD
- Once installed into the system, the component is not threatened anymore
- Therefore regular ESD requirements should hold for these components
  - AEC Q100 specifies HBM & CDM methods like in other non-automotive applications
  - No specific additional requirement for MM

Automotive Design Applications

- In the automotive world, product pins directly interfacing with the outside world (battery monitors, airbag sensors) may see another type of ESD threat
- This is the so-called system level ESD
- Since the IEC 61000-4-2 does not apply for pins, the automotive world recognizes specific standards
  - ISO 10605, which contains a part on modules (inside or outside the car)
  - University of Zwickau developed a test for bus pins of the CAN and LIN transceivers
  - IEC TS 62228 is a public procedure detailing the Zwickau method for CAN transceivers
  - These are only required for relevant pins in these type of applications

Conclusions for Automotive Applications

- It is now generally recognize that automotive products and consumer products alike need to be qualified for the same required ESD levels that include HBM and CDM
- Machine Model ESD specifications, that have remained as traditional for a long time, do not add any value for automotive ESD qualification
- In fact some scenarios, where bipolar like pulses may occur during car assembly, are best addressed by meeting the ISO requirements; but not through MM specifications
- All of these arguments against the MM, given throughout this presentation, apply equally to automotive applications
- “Zero Defects” are best addressed by the EOS failure conditions; not through MM qualification